

(NASA-CR-150218) DESIGN, FABRICATION, AND  
EVALUATION OF CHARGE-COUPLED DEVICES WITH  
ALUMINUM-ANODIZED-ALUMINUM GATES Interim  
Report (Mississippi State Univ.) 64 p  
HC A04/MF A01

N79-25316

CSCL 09C G3/33 Unclas.  
26855

NASA CONTRACTOR  
REPORT

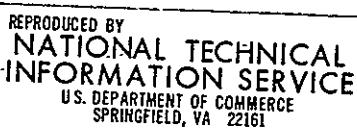
NASA CR-150218

DESIGN, FABRICATION, AND EVALUATION OF CHARGE-COUPLED  
DEVICES WITH ALUMINUM-ANODIZED-ALUMINUM GATES

By J. D. Gassaway and W. H. Causey, Jr.  
Department of Electrical Engineering  
Engineering and Industrial Research Station  
Mississippi State University  
State College, Mississippi 39762

February 1977

Interim Report



Prepared for

NASA - GEORGE C. MARSHALL SPACE FLIGHT CENTER  
Marshall Space Flight Center, Alabama 35812

NOTICE

THIS DOCUMENT HAS BEEN REPRODUCED  
FROM THE BEST COPY FURNISHED US BY  
THE SPONSORING AGENCY. ALTHOUGH IT  
IS RECOGNIZED THAT CERTAIN PORTIONS  
ARE ILLEGIBLE, IT IS BEING RELEASED  
IN THE INTEREST OF MAKING AVAILABLE  
AS MUCH INFORMATION AS POSSIBLE.

## TECHNICAL REPORT STANDARD TITLE PAGE

1. REPORT NO. NASA CR-150218	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.
4. TITLE AND SUBTITLE Design, Fabrication, and Evaluation of Charge-Coupled Devices with Aluminum-Anodized-Aluminum Gates		5. REPORT DATE February 1977
		6. PERFORMING ORGANIZATION CODE
7. AUTHOR(S) J. D. Gassaway and W. H. Causey, Jr.		8. PERFORMING ORGANIZATION REPORT #
9. PERFORMING ORGANIZATION NAME AND ADDRESS Department of Electrical Engineering, Mississippi State Univ. Engineering and Industrial Research Station State College, Mississippi 39762		10. WORK UNIT NO.
		11. CONTRACT OR GRANT NO. NAS8-26749
		13. TYPE OF REPORT & PERIOD COVERED Interim Contractor Report
12. SPONSORING AGENCY NAME AND ADDRESS George C. Marshall Space Flight Center National Aeronautics and Space Administration Marshall Space Flight Center, Alabama 35812		14. SPONSORING AGENCY CODE
15. SUPPLEMENTARY NOTES		
16. ABSTRACT A 4-phase, 49 1/2 bit CCD shift register was designed and fabricated using two levels of aluminum metallization with anodic $Al_2O_3$ insulation separating the layers. Test circuitry was also designed and constructed. A numerical analysis of an MOS-RC transmission line was made and results are given to characterize performance for various conductivities. The electrical design of the CCD included a low-noise dual-gate input and a balanced floating diffusion output circuit. Metallization was accomplished both by low voltage DC sputtering and thermal evaporation. The anodization was according to published procedures using a buffered tartaric acid bath. Approximately 20 wafers were processed with 50 complete chips per wafer. All devices failed by shorting between the metal levels at some point. Experimental procedures eliminated temperature effects from sintering and drying, anodic oxide thickness, edge effects, photoresist stripping procedures, and metallization techniques as the primary causes of failure. It was believed from a study of SEM images that protuberances (hillocks) grow up from the first level metal through the oxide either causing a direct short or producing a weak, highly stressed insulation point which fails at low voltage. The cause of these hillocks is unknown; however, they have been observed to grow during temperature excursions to $470^{\circ}C$ . There are subtleties in the metal preparation which have not been reported if this technique can be made to work or else the previously reported devices resulted from very low yield processes. It is recommended that the metal should never be heated during processing after it is deposited for anodization. Further research is necessary to describe preparation procedures for two-level metallization with an anodic oxide insulator.		
17. KEY WORDS		
19. SECURITY CLASSIF. (of this report) Unclassified	20. SECURITY CLASSIF. (of this page) Unclassified	

#### ACKNOWLEDGEMENTS

The cooperation of the technical and management personnel at Marshall Space Flight Center in making fabrication facilities available for certain portions of this work is gratefully acknowledged. This response contributed not only to the research efforts but also to the educational development of students who were involved.

## TABLE OF CONTENTS

Section	Page
ABSTRACT . . . . .	i
ACKNOWLEDGEMENTS . . . . .	ii
LIST OF FIGURES . . . . .	v
1. INTRODUCTION . . . . .	1
1.1 Systems Requirements . . . . .	1
1.2 Fabrication Considerations . . . . .	2
1.3 Performance Considerations . . . . .	3
2. ELECTRICAL DESIGN . . . . .	9
2.1 Charge Transfer Structure . . . . .	9
2.2 Input Gating . . . . .	16
2.3 Output Gating . . . . .	21
2.4 Test Devices and Circuits . . . . .	21
3. FABRICATION PROCEDURE . . . . .	26
3.1 Anodization Procedure . . . . .	26
3.2 Fabrication Schedule . . . . .	29
A. Wafer Clean . . . . .	29
B. Field Oxide Growth . . . . .	29
C. N <sup>+</sup> Diffusion Cutout . . . . .	31
D. N <sup>+</sup> Predeposition at 980°C . . . . .	31
E. N <sup>+</sup> Drive-in at 1200°C . . . . .	33
F. P <sup>+</sup> Diffusion Cutout . . . . .	33
G. P <sup>+</sup> Predeposition at 980°C . . . . .	33
H. Gate Oxide Cutout . . . . .	35
I. Gate oxidation at 1200°C . . . . .	35
J. First Aluminum . . . . .	35
K. First Aluminum Etch . . . . .	37
L. Aluminum Anodization . . . . .	37
M. Aluminum Oxide Etch . . . . .	37
N. Aluminum Bus Line Etch . . . . .	40
O. Ohmic Contact Cutout . . . . .	40
P. Second Aluminum Deposition . . . . .	42
Q. Second Aluminum Etch . . . . .	42
R. Optional Passivation Step . . . . .	42

TABLE OF CONTENTS (Continued)

Section	Page
4. EVALUATION AND MODIFICATIONS . . . . .	45
4.1 Initial Run . . . . .	45
4.2 Thermally Evaporated Aluminum . . . . .	46
4.3 Additional Runs with Sputtered Aluminum . . . . .	47
4.4 SEM Inspections . . . . .	47
5. SUMMARY AND CONCLUSIONS . . . . .	53
REFERENCES . . . . .	57

LIST OF FIGURES

Figure	Page
1.1 Model for MOS-RC transmission line . . . . .	6
1.2 Voltage profiles on MOS-RC transmission line with one end open and step input. . . . .	7
1.3 Normalized time vs. ratio of voltage at open end of line to input voltage for an MOS-RC transmission line . . . . .	8
2.1 Basic 4-phase CCD structure with $\text{Al}_2\text{O}_3$ . . . . .	10
2.2 Surface potential vs. reduced gate voltage for an MOS structure . . . . .	11
2.3 Surface potential profiles during charge transfer for 4-phase CCD . . . . .	13
2.4 Clock waveforms for the transfer electrodes for the 4-phase CCD . . . . .	14
2.5 Charge transfer inefficiency vs. normalized time for charge transfer limited by diffusion and self fields <sup>7</sup> . .	15
2.6 Modulation transfer function (MTF) for operation of the CCD as a delay line with a sinusoidal input signal for clock frequencies of 2 and 10 MHz . . . . .	17
2.7 Surface potential profiles illustrating the loading of charge at the input . . . . .	18
2.8 (a) Connection diagram for operation of input and transfer circuits (b) Circuit diagram for clamped inverter indicated in (a) . . . . .	20
2.9 Surface potential profiles illustrating operation of output circuit . . . . .	22
2.10 Circuit schematic for output detector and output waveform . . . . .	23
2.11 Four phase waveform generator adapted from reference 3 . . . . .	25
3.1 Photomicrograph of 4-phase CCD with $\text{Al}-\text{Al}_2\text{O}_3$ insulated gates . . . . .	27

LIST OF FIGURES (Continued)

Figure	Page
3.2 Plot of measured anodization current for wafer with devices . . . . .	28
3.3 First mask level . . . . .	30
3.4 Second mask level . . . . .	32
3.5 Third mask level . . . . .	34
3.6 Fourth mask level . . . . .	36
3.7 Fifth mask level . . . . .	38
3.8 Sixth mask level . . . . .	39
3.9 Seventh mask level . . . . .	41
3.10 Eighth mask level . . . . .	43
3.11 Ninth mask level (optional) . . . . .	44
4.1 SEM image of unsintered sputtered aluminum on $\text{SiO}_2$ and sputtered, sintered aluminum . . . . .	48
4.2 SEM image of unsintered, sputtered aluminum on sintered aluminum and anodic $\text{Al}_2\text{O}_3$ on sintered aluminum . . . . .	49
4.3 Stepped SEM image of unsintered, sputtered aluminum on anodic $\text{Al}_2\text{O}_3$ on sintered aluminum . . . . .	50
4.4 Normal SEM image of unsintered, sputtered aluminum on anodic $\text{Al}_2\text{O}_3$ on sintered aluminum . . . . .	51

## 1. INTRODUCTION

The objective in this work was to construct and evaluate CCD's with Al-anodized  $Al_2O_3$  insulated gates in a dynamic memory application for the DELTIC-DFPCC correlator which was constructed in previous work. An anodic oxidation procedure was chosen which had been patented by Texas Instruments and reported in several publications.<sup>2,3,4</sup> The scheme has many attractive features, is well documented, and there were no reported difficulties. Therefore, this work represented an attempt at straightforward application of the method along with other established MOS technology to achieve a state of the art CCD design.

### 1.1 Systems Requirements

A nominal 50 bit (49 1/2) CCD was designed for cascaded operation of four CCD's and one or two D-flip-flops to achieve 199 or 200 bit shift registers. This degree of complexity was chosen in order to improve the process yield, since there was no experience with the anodization process on an LSI scale to draw upon.

The clock frequency for operation in this system is governed by:

$$f_c > 2pNW , \quad (1.1)$$

where  $p$  is the number of phases,  $N$  is the number of bits, and  $W$  is the bandwidth of the sampled signal. Although the presently breadboarded system was designed as a demonstration vehicle and has not operated at a high frequency, the general application of CCD's to the DELTIC-DFPCC will tax CCD performance to the ultimate in speed requirement, since this is the

most highly stressed part of the system from the standpoint of speed. The input rate to the DELTIC in the breadboard system is limited by CMOS IC packages; however, for the 200 bit DELTIC, the ultimate speed that can be demanded exceeds the fastest CCD reported (100 Mhz)<sup>5</sup> by a factor of 20.

In this design, it was considered desirable that the CCD operate compatibly with CMOS, and, since the devices would represent a unique opportunity for experimentation, it was desirable that they operate with good linearity and low noise performance in analog delay line applications.

## 1.2 Fabrication Considerations

One advantage of the anodic aluminum oxide insulation scheme is its simplicity as compared with the polysilicon gate schemes or the gapped structures requiring ion implanted distributions of doping impurities in the channel. The bucket-brigade device is simpler than any of the CCD schemes but suffers with respect to charge transfer efficiency and ultimate operating speed. The polysilicon gate procedure requires CVD and/or thermal processing to achieve insulation between the overlapping aluminum and polysilicon phase electrodes. During thermal growth of an insulating oxide, hydrogen enhanced diffusion of the polysilicon dopant through the channel oxide causes problems. Good etch definition of the polysilicon can be a problem in the overlapping structure. Gapped, ion-implanted structures require two different implantations, and the alignment of one of these distributions in the channel is critical.

The main disadvantage of anodic aluminum in LSI structures is that it is not well established as a reliable insulator compatible with IC processing. Most of the reported progress has been achieved within one company.<sup>2,3,4</sup> Recent reports elsewhere<sup>6</sup> deal with situations not involving a large number

of devices. In this work, a p-channel technology was chosen in which fabrication required only furnace processing, metallization and anodization in a low temperature bath. A minimum of 7 mask levels are required for photoengraving, although 8 were actually used in this work.

### 1.3 Performance Considerations

One of the first considerations for any MOS technology is to prevent the channel oxide from being exposed to charge contamination which extraneously induces channel conduction and produces drift and erratic behavior which are undesirable. Therefore, the all aluminum gate, overlapping electrode structure is superior in this regard to the gapped CCD structures.

In the target application for the devices designed, speed of operation and large bit storage are quite important. For the ultimate limit in application, the surface channel CCD would not be satisfactory and buried channel<sup>7</sup> (peristaltic<sup>5</sup>) devices would be required. However, it has been recognized that RC transmission line effects can also become a limiting factor. If there is sufficient delay on the line, then bits furthest from the clock source end of the line will not be shifted at the proper time. One solution is to use a multiply fed line for driving the phases; however, a simpler solution is to use a conducting line with sufficiently low resistivity to preclude significant delay.

A model of an RC transmission line is shown in Figure 1.1 which will be analyzed with a one-dimensional model which assumes the line is uniform. A practical line can be treated simply enough by incorporating an averaging procedure to account for periodic parametric variations, since the line is governed by dispersion effects and will not show stop-band-pass band effects that a loss-less line with periodic parameters will

show. In the simplified model, the silicon substrate is treated as a ground plane, which leads to a partial differential equation for voltage vs. time and distance given by:

$$RC_T \frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2} \quad (V/cm^2) \quad (1.2)$$

$$C_T = \frac{C_{OX} C_S}{C_{OX} + C_S} = \begin{cases} \frac{C_{OX}}{[1 + \alpha(V - V_T)]^{1/2}} & , \quad V > V_T \\ C_{OX} & , \quad V \leq V_T \end{cases} \quad (1.3)$$

$$\alpha = \frac{2\epsilon_{OX}^2 \epsilon_0}{qN_B \epsilon_S t_{OX}^2} \quad , \quad (\text{volt}^{-1}) \quad (1.4)$$

$$R = e/t_c \quad , \quad (\text{ohms}) \quad (1.5)$$

where the symbols are standard and defined in the glossary of terms. When the voltage on the line is less than the threshold  $V_T$ , equation (1.2) is simply the linear diffusion equation, and for a unit step voltage input at  $x = 0$  on a semi-infinite line, the voltage profile on the line is described by:

$$V(x, t) = \text{erfc}(\sqrt{RC_T} x/\sqrt{t}) \quad . \quad (1.6)$$

For the more general non-linear case, equation (1.2) can be solved by finite difference techniques.<sup>8</sup> In such an analysis, it is convenient to define a normalized time by

$$\tau = \alpha L^2 \rho C_{OX} / t_c \quad (1.7)$$

where  $\alpha$  is a parameter related to the discretization of the problem.

Figure (1.2) shows voltage profiles on a finite line with one end open for voltages at and exceeding the threshold value. Figure (1.3) shows the voltage at the end of the line vs.  $t/\tau$  for various ratios of the applied to threshold voltage. The rise times; defined as the time required to reach 90% of the steady value, are indicated on the curves for computations in which  $\alpha = 10$  was used. Taking  $\rho/t_c = 1$  ohm and  $C_{OX} = 3.45 \times 10^{-8} \text{ f/cm}^2$  corresponding to a  $100^\circ \text{A}$  oxide:

$$\tau \geq 34.5 L^2 \text{ nsec} \quad (1.8)$$

where  $L$  is the line length in cm. For the CCD fabricated in this work  $L \sim 0.1$  cm, and the delay is less than 0.345 nsec, which would not be a limiting factor for the surface channel CCD. For a line four times as long, or with a sheet resistance of 16 ohms, the delay would be 5 nsec which would be a significant factor for high speed buried-channel devices ( $> 100$  MHz). Therefore, the use of all aluminum lines would be advantageous.

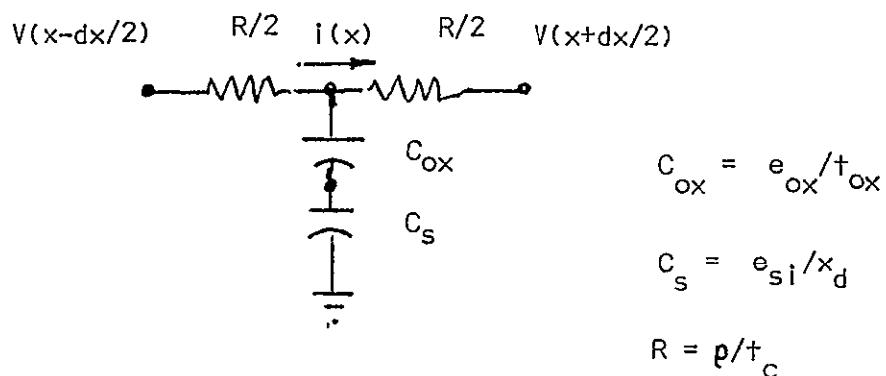
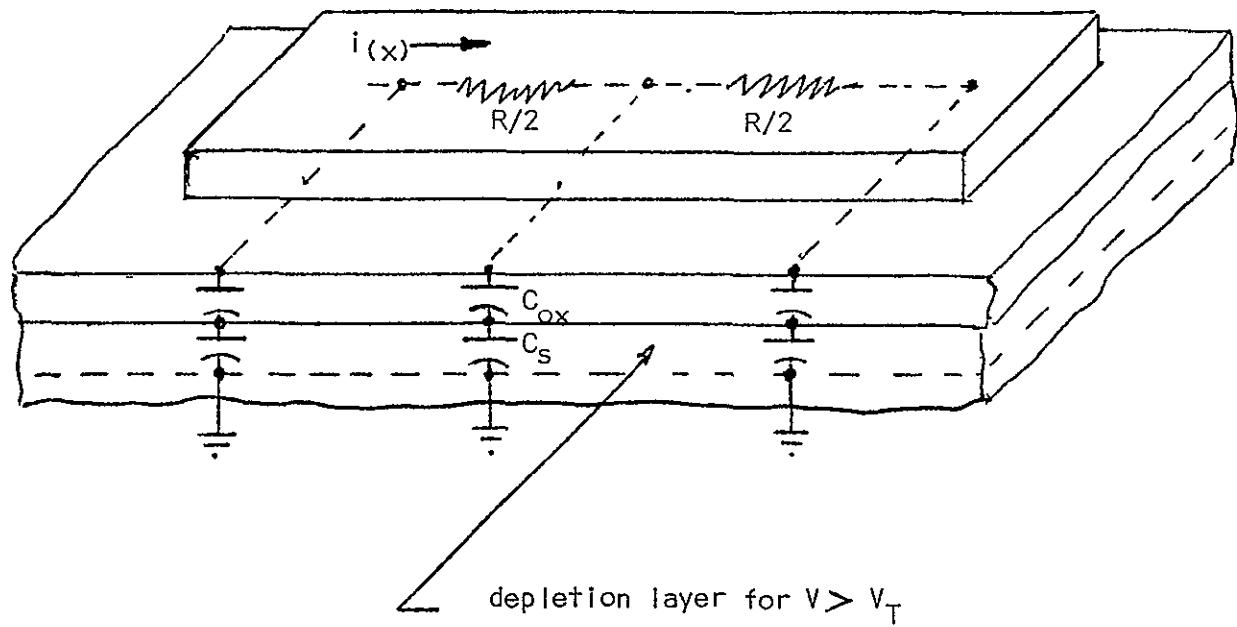


Figure 1.1 Model for MOS-RC transmission line.

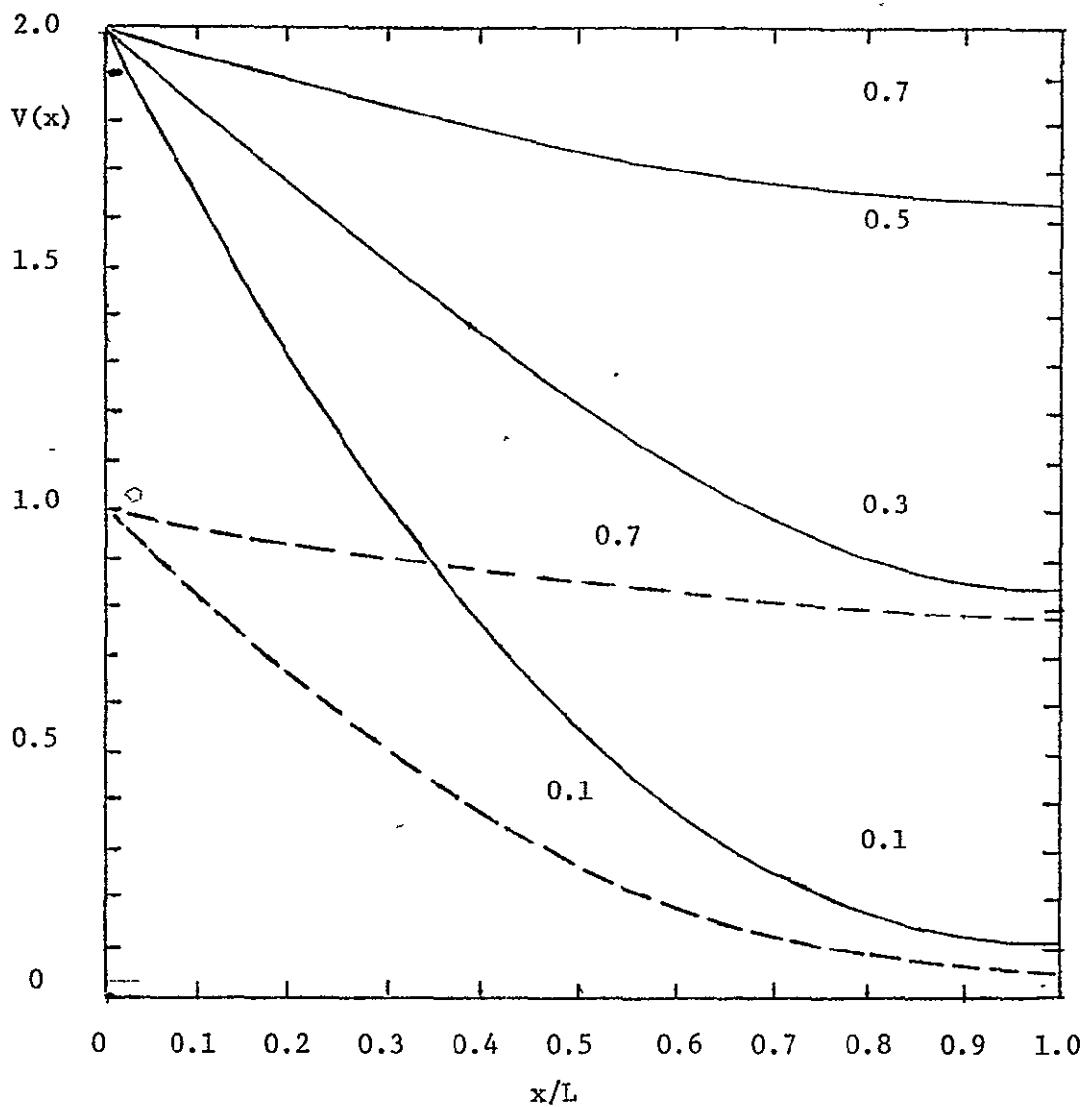


Figure 1.2 Voltage profiles on MOS-RC transmission line with one end open and step input.

Solid curves:  $V_{in} = 2V$ , above threshold.

Dashed curves:  $V_{in} = 1V$ , just at threshold.

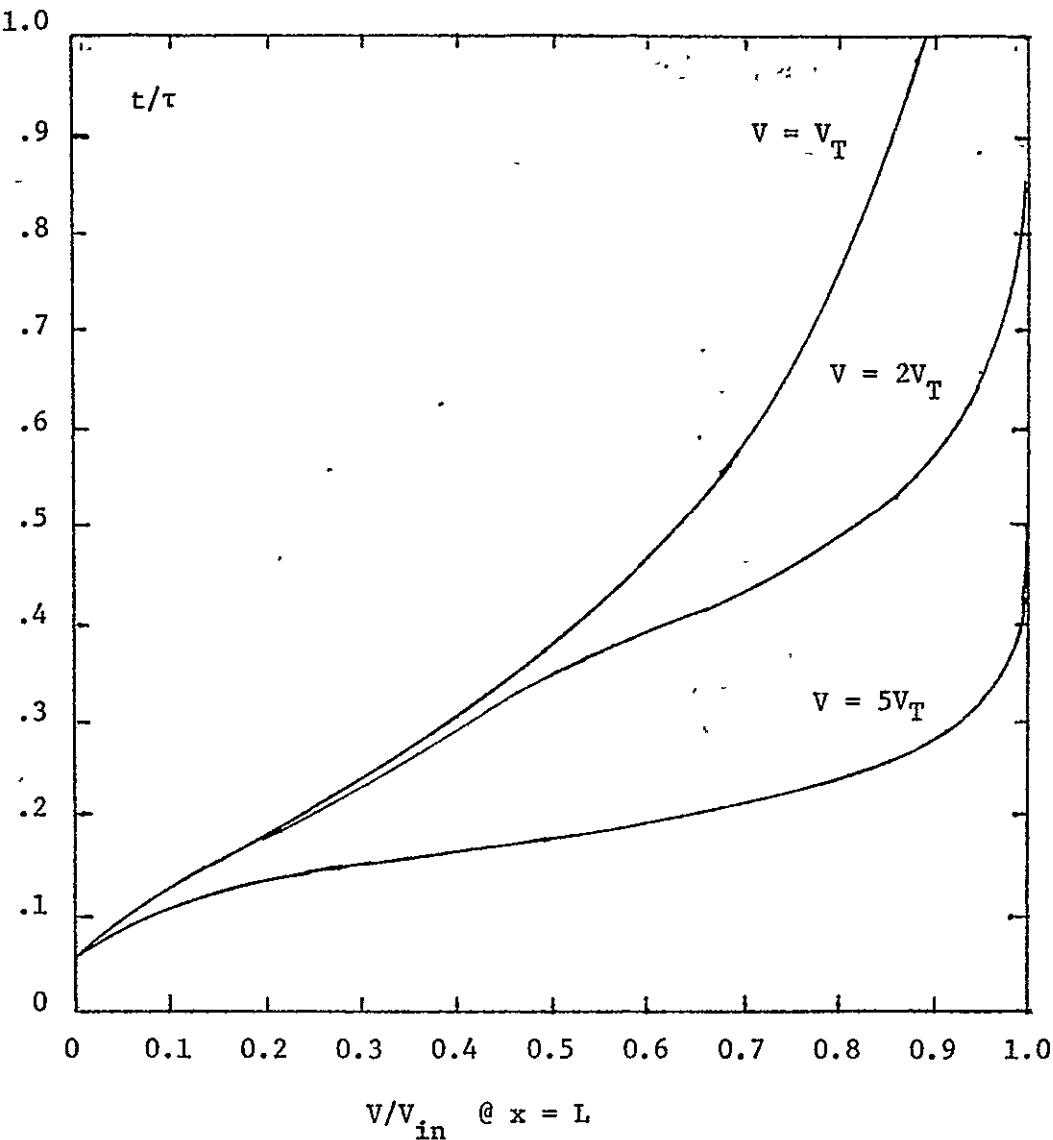


Figure 1.3 Normalized time vs. ratio of voltage at open end of line to input voltage for an MOS-RC transmission line.

$$\tau = 10L^2 C_{ox} / t_c$$

$t_c$  = conductor thickness.

$C_{ox} = 3.45 \times 10^{-8} \text{ f/cm}^2$  for  $t_{ox} = 1000\text{\AA}$

$\rho$  = conductor resistivity.

$V_T$  = threshold voltage, 1V.

## 2. ELECTRICAL DESIGN

The CCD was designed for 4-phase operation which allowed fabrication with only one anodization step. A dual input gate was incorporated which allows for linear, low noise operation of the device for analog delay line applications. The output circuit was designed with a floating diffusion detector, and a dummy diffusion was also incorporated which, with a pair of source followers, allows operation as a balanced, gated charge integrator. Therefore, the devices could also be evaluated in analog delay line applications.

### 2.1 Charge Transfer Structure

The basic 4-phase cell is illustrated in Figure 2.1. A one-dimensional analysis of the surface potential vs. gate voltage is valuable for design purposes. The one dimensional model for an N-type substrate gives the surface potential,  $\psi_s$ , in terms of the reduced gate voltage,  $v'_G$ , as:

$$\psi_s = v'_G - v_1 + \sqrt{v_1^2 - 2v_1 v'_G} \quad (2.1)$$

where,

$$v'_G = v_G - v_{FB} - v_{sub} + Q/C_{OX} , \quad (2.2)$$

$$v_1 = qN_d \epsilon_s / C_{OX}^2 , \quad (2.3)$$

and,

$$v_{FB} = -Q_{SS}/C_{OX} + \phi_{MS} , \quad (2.4)$$

where the notation is standard and is defined in the glossary. The fabrication procedure used was a thick oxide p-channel MOS process with

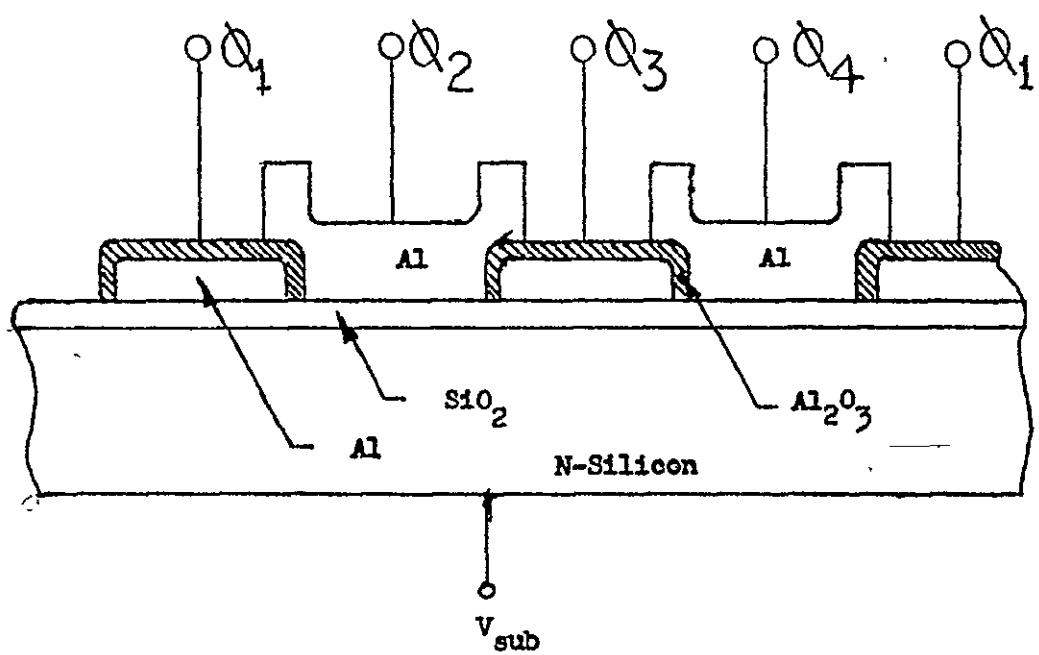


Figure 2 .1 Basic 4-phase CCD structure with  $\text{Al}_2\text{O}_3$  insulation between levels.

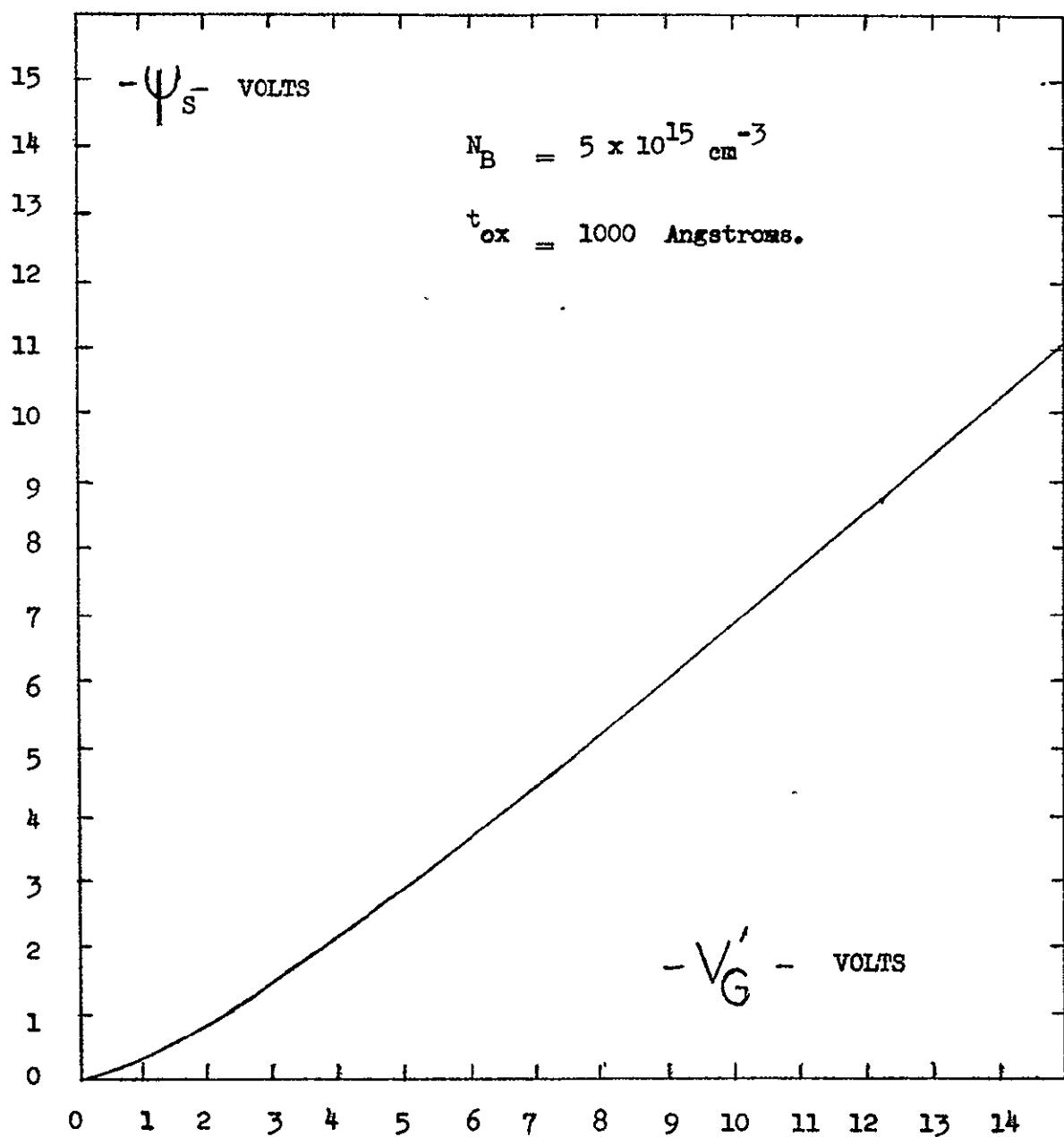


Figure 2 .2 Surface potential vs. reduced gate voltage  
for an MOS structure.

1000 Å channel oxide thickness. The substrate doping is  $\sim 5 \times 10^{15} \text{ cm}^{-3}$  and the flatband voltage achieved is typically  $V_{FB} \sim \text{V}$ . Calculated results are shown in Figure 2.2 for equation (2.1), and it is seen that the relationship between the surface potential and reduced gate voltage is almost linear. It is assumed that the device will be operated with a substrate bias ( $V_{sub}$ ) which exceeds the flatband voltage by approximately 1 V so that a gate voltage of - 10 V produces a surface potential of  $\sim - 7.7 \text{ V}$ . Figure 2.3 illustrates the surface potential profiles for a pull-push sequence of operation by the transfer phases for accomplishing charge transfer. Idealized waveforms for the clock phases driving the transfer gates are shown in Figure 2.4. Approximately half of the charge is transferred after the succeeding phase electrode goes negative, and the rest of the charge is transferred on the trailing edge of the phase voltage waveform. The inefficiency of the charge transfer depends upon the overlap of the phases.

The worst case for the charge transfer time required occurs when the fringing field is negligible and the charge transfer dynamics are limited by diffusion. Figure 2.5 shows the charge transfer inefficiency,  $\epsilon$ , vs. the normalized time. It is assumed that the required charge transfer efficiency (CTE) corresponds to a transfer time,  $t_T$ , given by:

$$t_T = 15 L^2/\mu . \quad (2.5)$$

For a transfer structure with gate width  $L = 0.4 \text{ mil}$  and operation with holes in a p-channel, the time required is  $t_T \sim 77 \text{ nsec}$ . Referring to Figure 2.5, it is obvious that the charge begins to transfer quite rapidly when the succeeding phase goes negative. Therefore, almost half of the charge will be transferred before the phase voltage begins to rise.

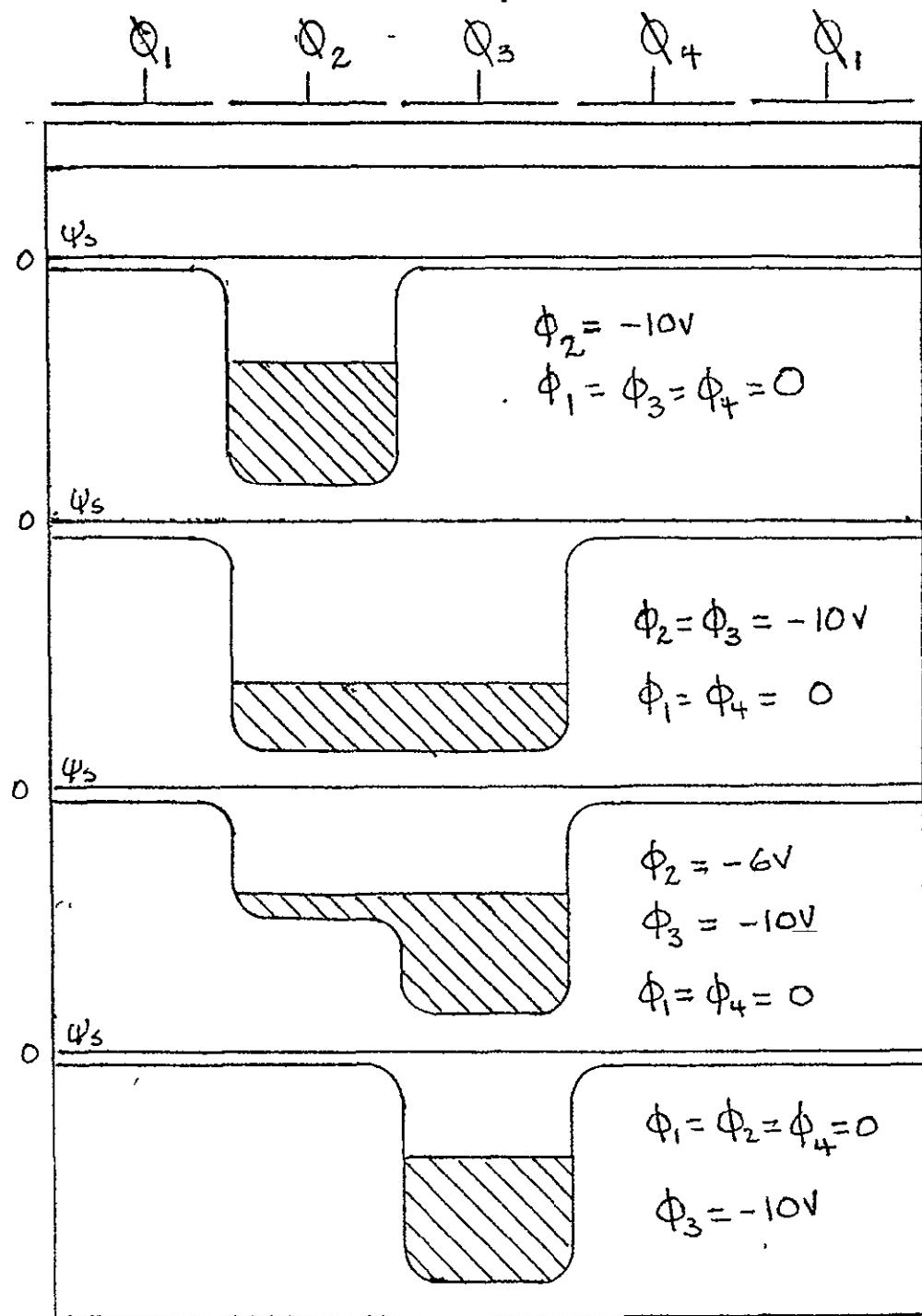


Figure 2.3 Surface potential profiles during charge transfer for 4-phase CCD.

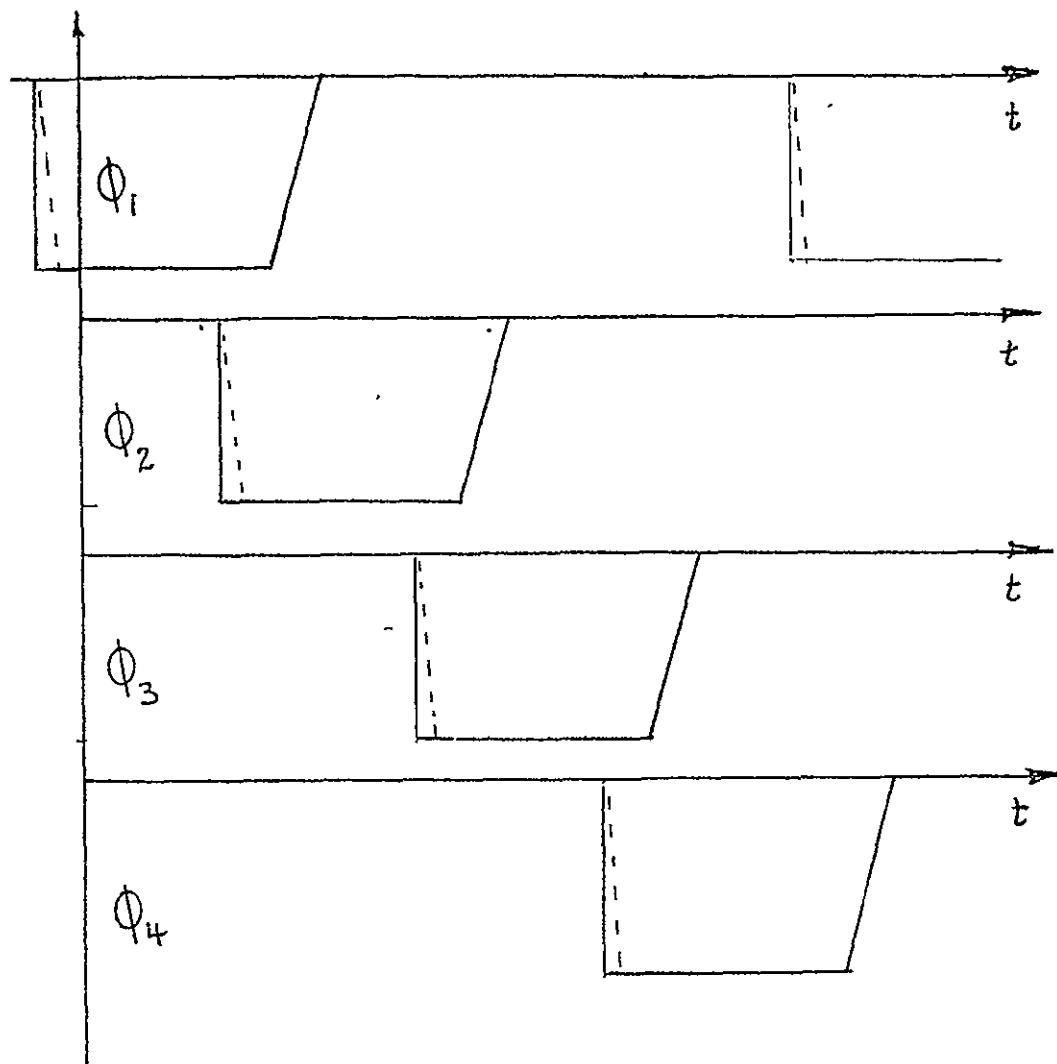


Figure 2.4 Clock waveforms for the transfer electrodes  
for the 4-phase CCD.

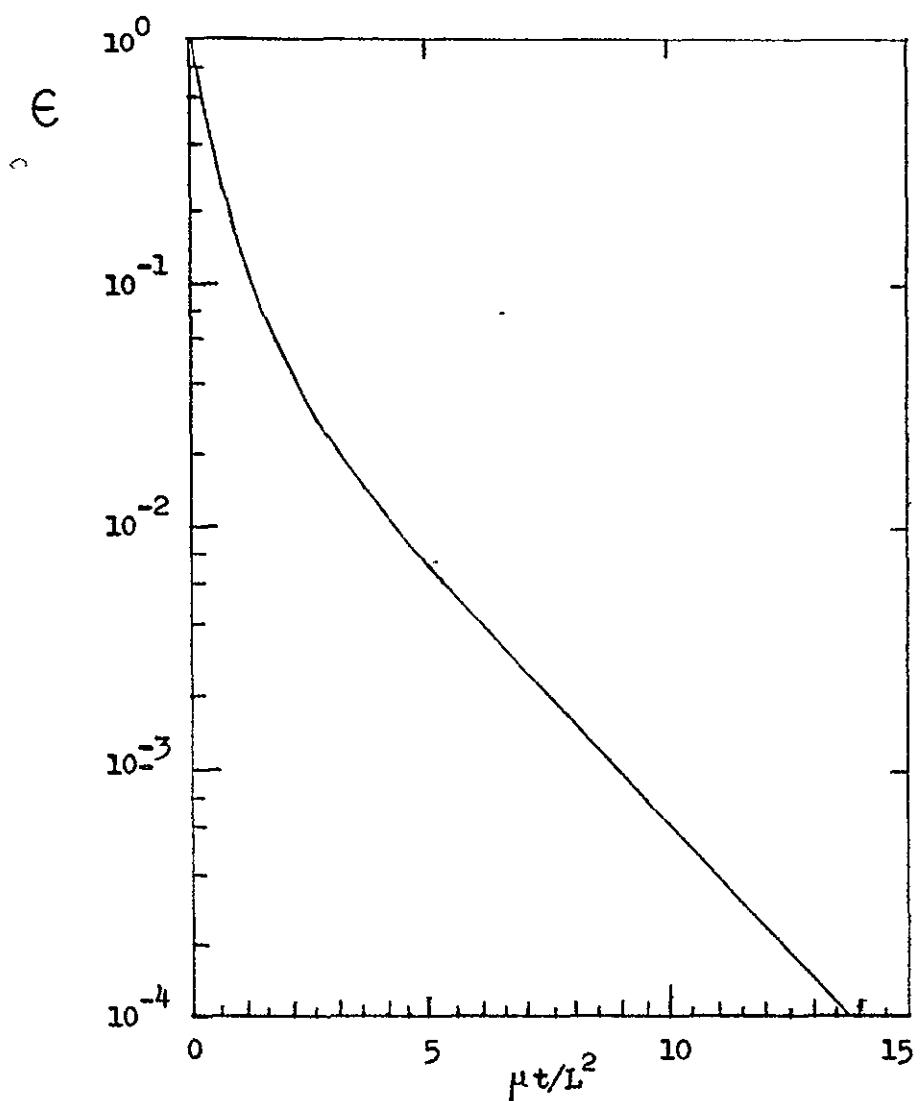


Figure 2.5 Charge transfer inefficiency vs. normalized time for charge transfer limited by diffusion and self fields.<sup>7</sup>

Again, the remaining charge begins to transfer rapidly during the beginning of the trailing edge and then slows. The total overlap time required is, on the order of 100 nsec, of which approximately 75% should be allotted to the trailing edge. A conservative estimate of the required clock period is  $T > 4 \times 2 \times 100$  nsec; however, the minimum clock period tolerable without reducing the time available for charge transfer is  $T \sim 4 \times 100$  nsec, where the factor 4 comes from the number of phases and the factor 2 allows for almost full transfer during each half of the operation. The latter value limits the clock frequency to a maximum of  $f \sim 2$  MHz before the overlap begins to be reduced, thus lowering the CTE.

A parameter of interest for operation of the CCD as an analog delay line is the modulation transfer function (MTF) given by:<sup>10</sup>

$$MTF = \exp[-N\epsilon(1 - \cos(\pi f/f_c))] . \quad (2.6)$$

This is the ratio of the amplitude of a sampled sinewave at the output of a sampled sinewave at the output with respect to that of a sine wave input. For the operating and design parameters given in the preceding, the MTF is almost unity up to the Nyquist frequency for a clock frequency of 2 MHz. For operation at a clock frequency of 10 MHz, the time available for charge transfer would be cut by a factor of 5, thus increasing  $\epsilon$  to approximately  $10^{-2}$ . In this case, the MTF begins to roll-off more rapidly as shown in Figure 2.6.

## 2.2 Input Gating

The input charge is controlled by the two gates,  $G_1$  and  $G_2$ , and the input diode ID. A low noise, highly linear operating mode has been discussed in the literature<sup>11</sup> and is illustrated in Figures 2.7 and 2.8.

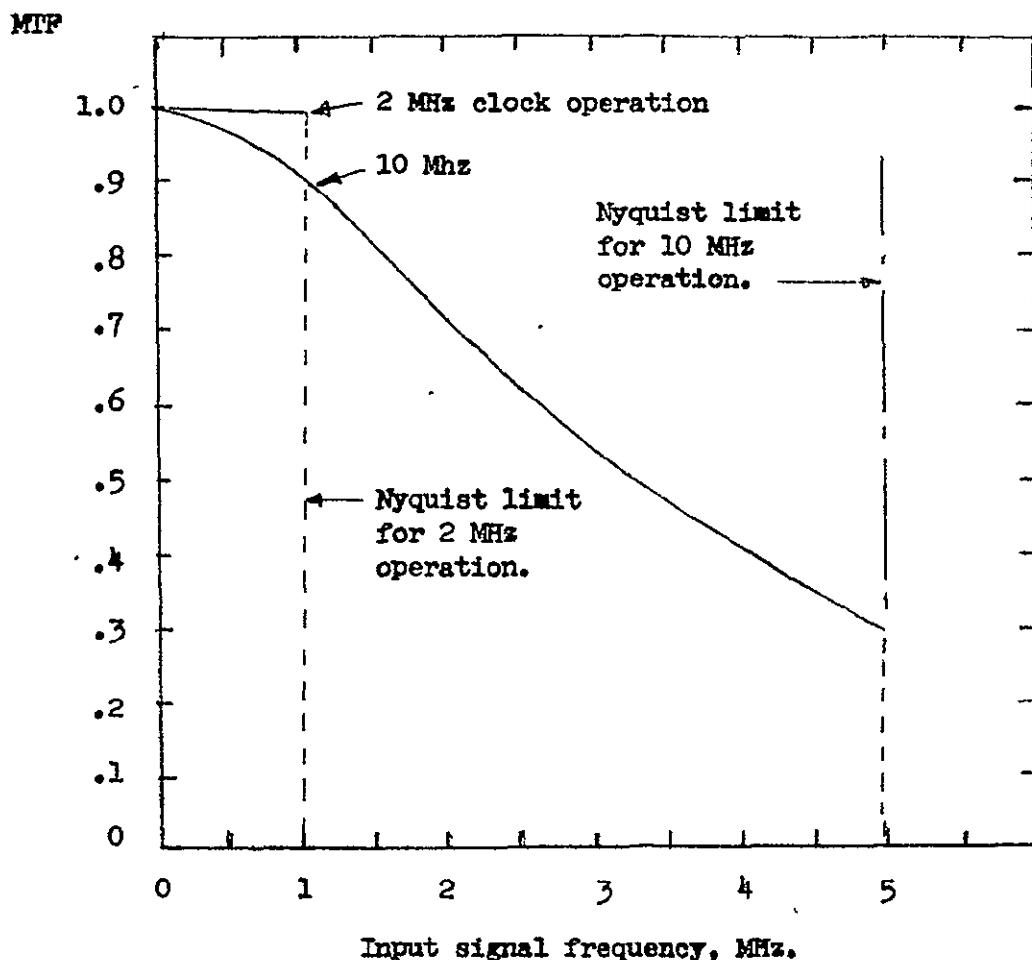


Figure 2.6 Modulation transfer function (MTF) for operation of the CCD as a delay line with a sinusoidal input signal for clock frequencies of 2 and 10 MHz.

ORIGINAL PAGE IS  
OF POOR QUALITY

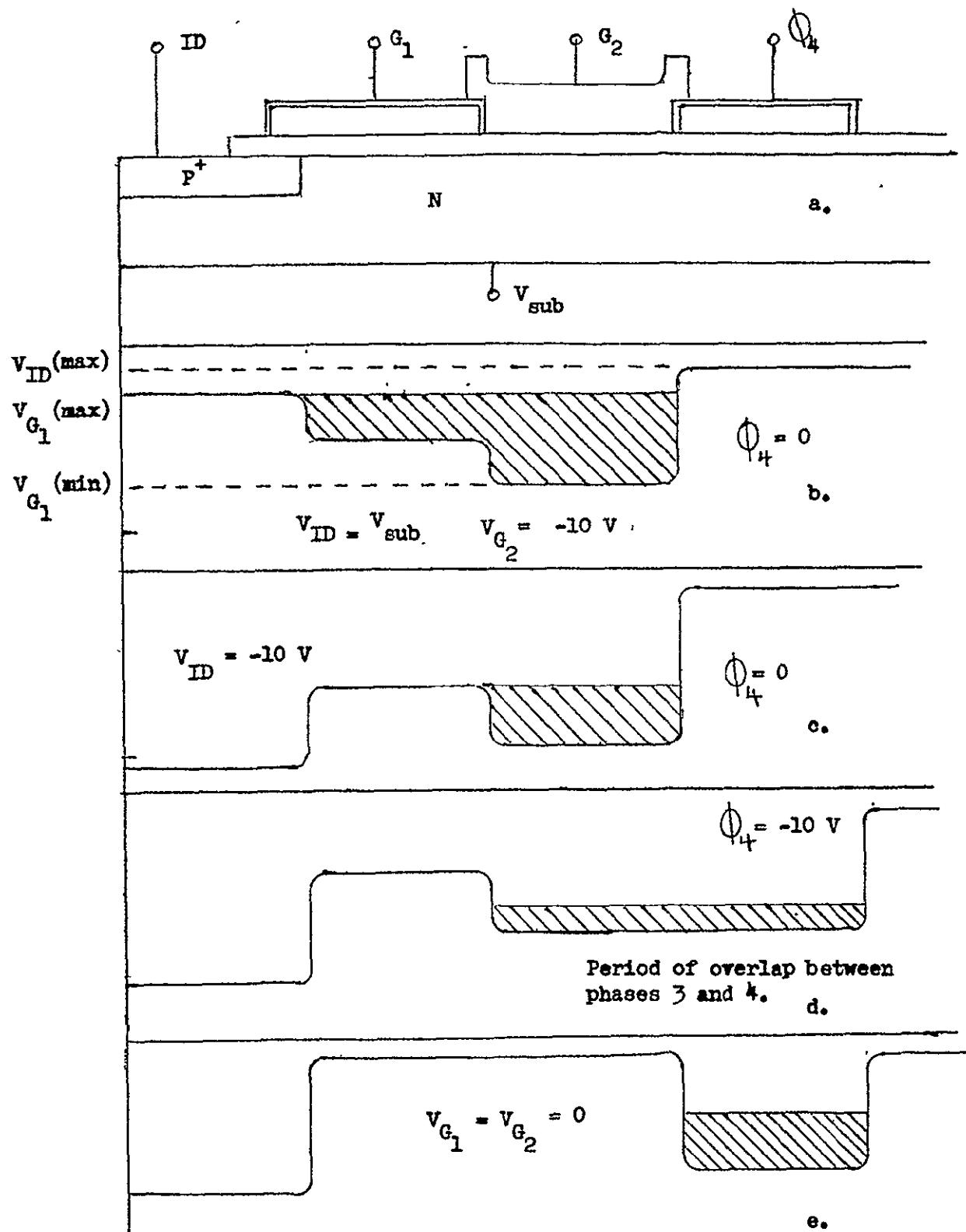


Figure 2.7 Surface potential profiles illustrating the loading of charge at the input. Sequence top to bottom; phase 2, phase 3, overlap of phase 3 and 4, and phase 4.

The sequence of operation is as follows:

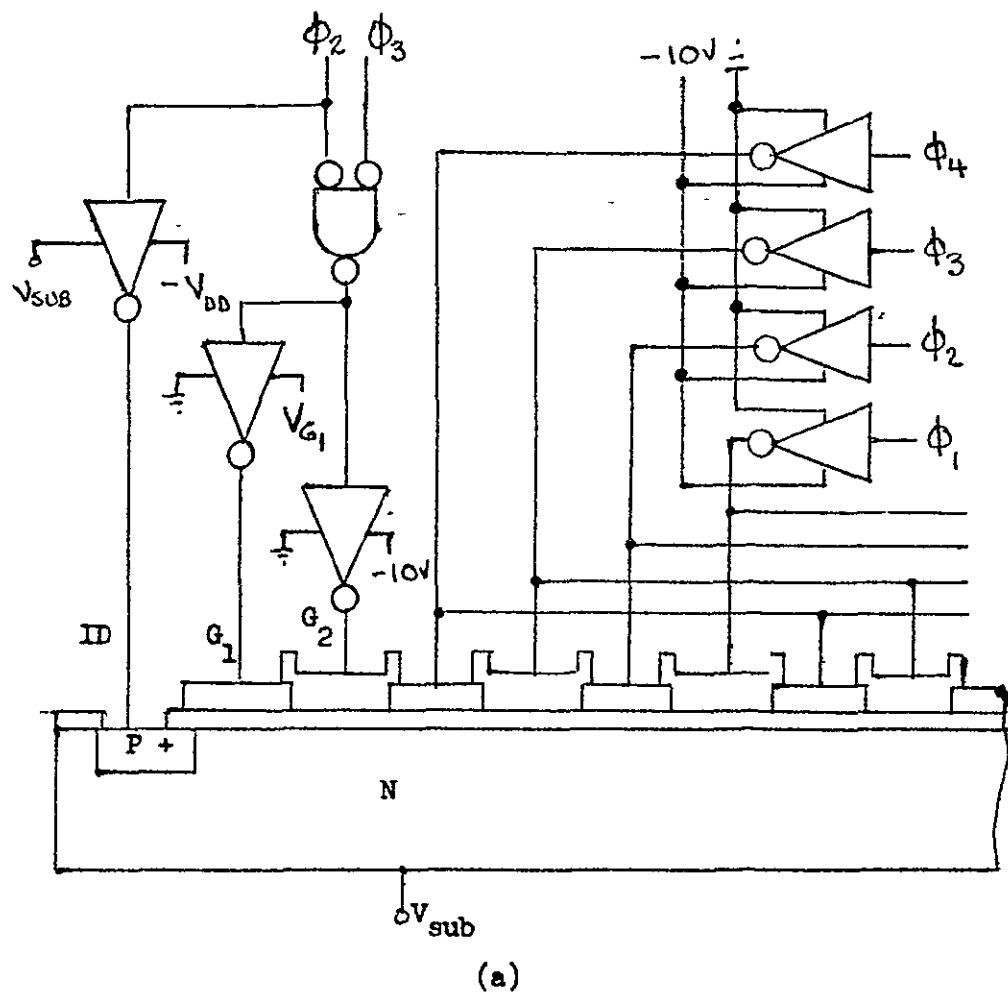
- (a) Gates  $G_1$  and  $G_2$  are pulsed on during phases 2 and 3.
- (b) The input diode is pulsed on during phase 2 flooding charge under the gates  $G_1$  and  $G_2$ . It is essential that the diode should not be pulsed beyond a value corresponding to the rest potential for the transfer electrodes ( $\sim -0.3V$ ). Assuming 0.6V for the junction bias  $V_{ID} \leq V_{sub} + .3V$ . If this value is exceeded, charge will be injected across  $G_1$  and  $G_2$  and down the channel causing misoperation; however, this condition is easily detected in operation.
- (c) During phase 3, the input diode is cut off and charge drains back from gates  $G_1$  and  $G_2$  leaving a trapped charge under  $G_2$  equal to:

$$Q = C_G(V_{G1} - V_{G2}) ,$$

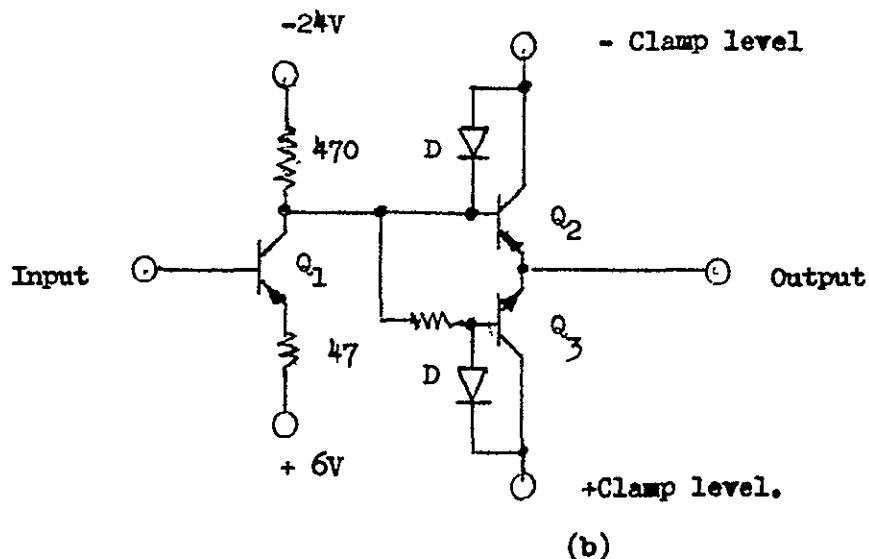
where  $C_G$  is the gate capacitance

- (d) Charge is transferred to the first phase 4 electrode during the overlap of phases 3 and 4.

The diagram in Figure 2.8 illustrates a test circuit for operation of the input devices in a pulsed mode as indicated in the preceding. The clamped drivers can be operated with DC or time varying inputs on the clamps for test purposes. It is possible to operate gate  $G_1$  with a direct negative input without switching; however, as phase 3 comes up to push charge from  $G_2$  to the first phase 4 electrode, some charge will be pushed backward. Therefore operation would not be quite as linear, although it would perhaps be satisfactory for many purposes.



(a)



(b)

Figure 2.8 (a) Connection diagram for operation of input and transfer circuits.  
 (b) Circuit diagram for clamped inverter indicated in (a).

### 2.3 Output Gating

The output gating structure is illustrated in Figures 2.9 and 2.10, with the latter giving a circuit representation of the gating action which occurs. For operation as a floating diffusion detector,<sup>12</sup> the following sequence holds:

- (a) During phase 1 charge is partially transferred to the floating diffusion (FD) which is biased negatively by a DC voltage on the electrode above the oxide. During the overlap of phase 1 and 2, the remaining charge is transferred, and the FD attains the maximum potential (which remains negative).
- (b) After the overlap of phases 1 and 2, the FD voltage is at full value and may be sampled. Sampling during the overlap would give a proportional, but attenuated, signal.
- (c) The reset electrode is pulsed negative during phase 3 or 4, and the FD is emptied into the drain, which should be at a negative bias approximately equal to that for the input diode.

In the gated charge integrator mode of operation,<sup>13</sup> the dummy diffusion is gated simultaneously with the FD detector. The only charge obtained is that due to thermal leakage and feedthrough from the reset gate. The differential output balances these bias components and yields an output proportional to the signal charge.

When operated as described in the preceding, the CCD give 49 1/2 bits of delay. For 199 or 200 bit operation in the DELTIC application, one or two D-flip-flops must be added.

### 2.4 Test Devices and Circuits

The chip design includes several test devices for evaluation of the process, which include:

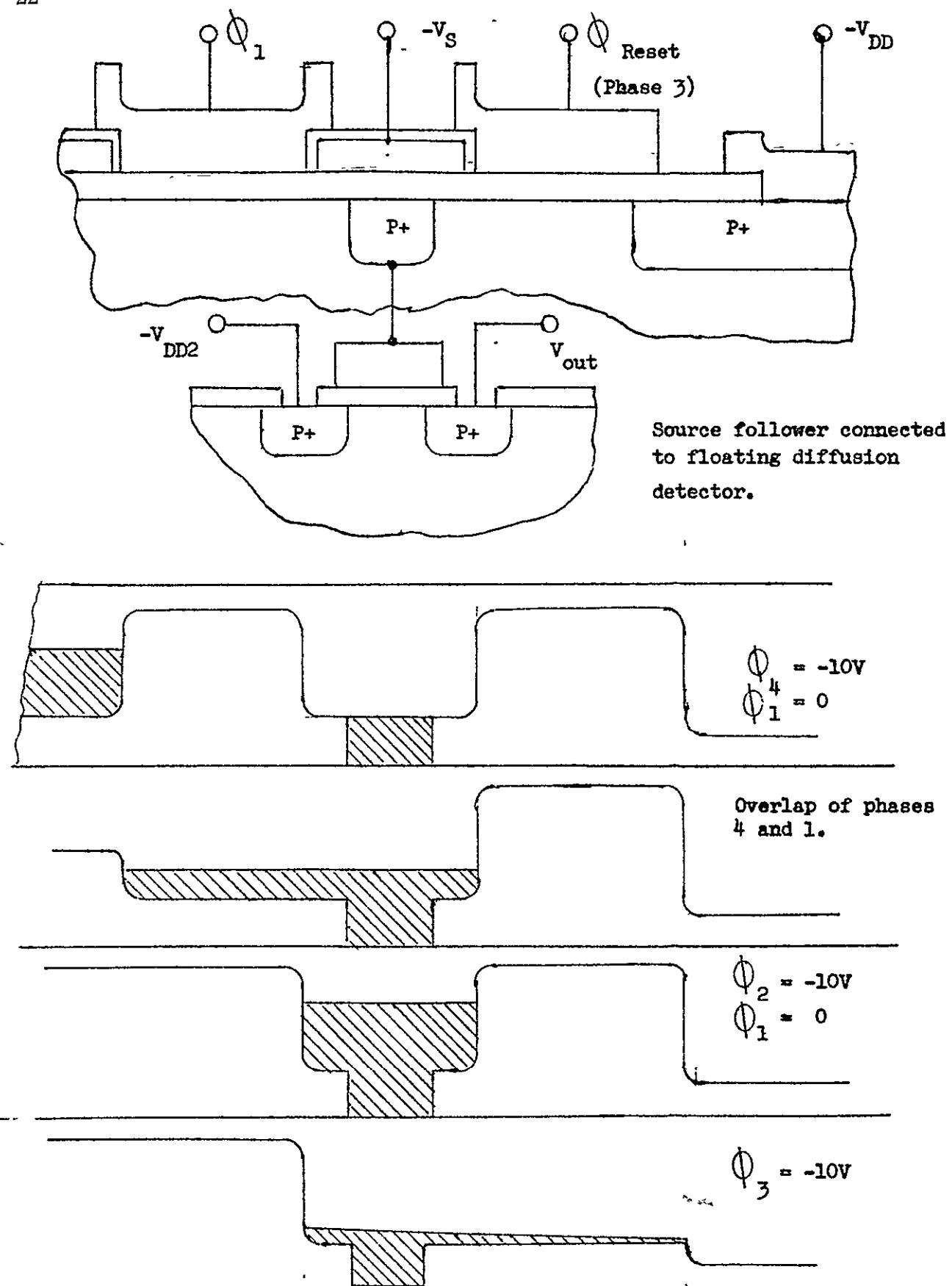


Figure 2.9 Surface potential profiles illustrating operation of output circuit.

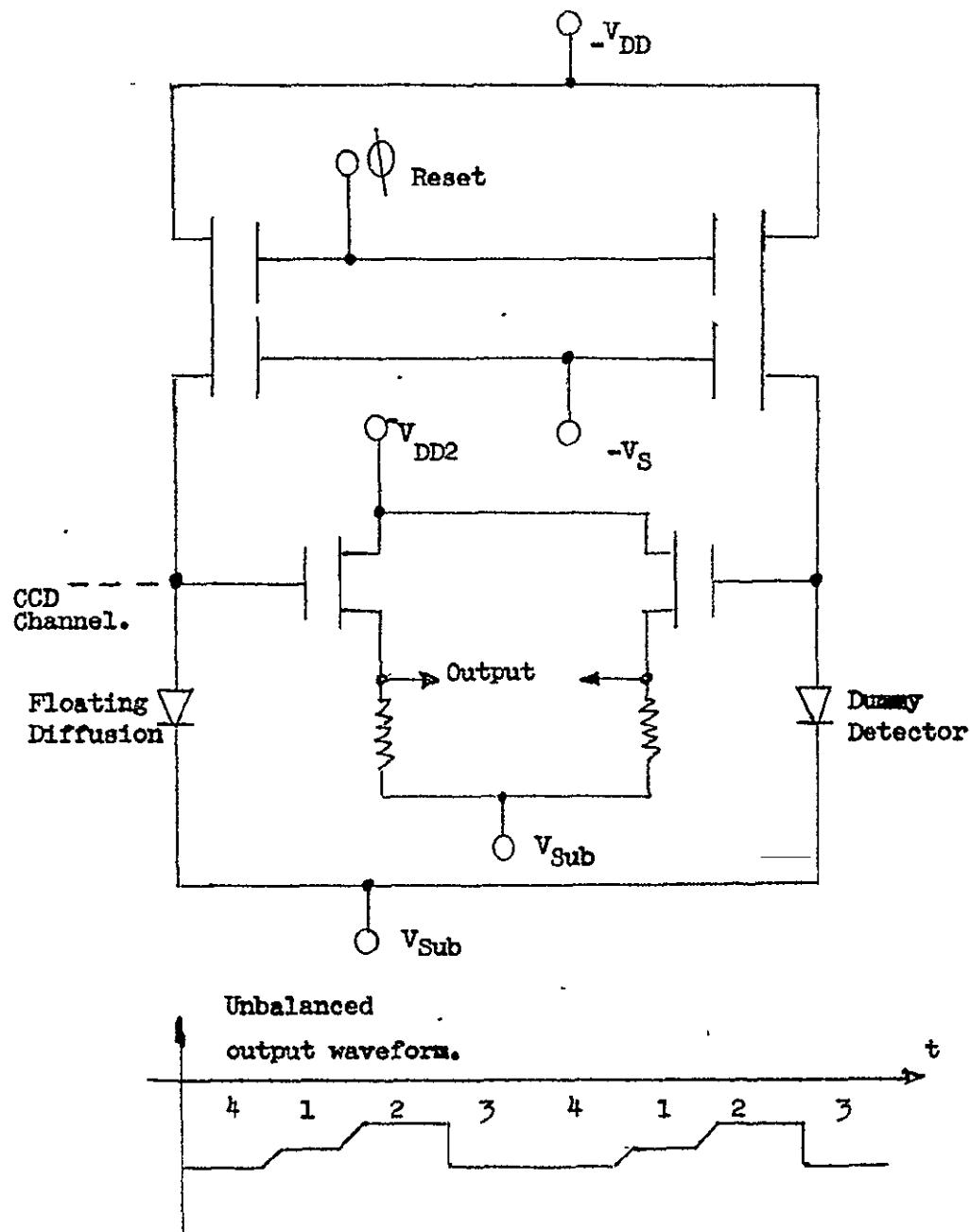


Figure 2.10 Circuit schematic for output detector and output waveform .

- (a) Finger patterns for destructive tests of the anodized aluminum insulation.
- (b) Capacitors for evaluating thickness, or dielectric constant and leakage current through the insulation.
- (c) MOS transistors for evaluating the flatband and threshold voltages achieved by the process.

The drivers for the input circuits and the transfer phases were constructed as illustrated in Figure 2.8-b. These drivers have a very fast fall time (< 20 nsec) and variable rise time (30 - 200 nsec). An integrated version would use MOS gates on a well laid out PC board or hybrid substrate; however, for flexibility in testing utilizing several boards, the low impedance TTL logic with bipolar drivers gives added convenience. A minimum of 6 drivers is required, in which case  $G_1$  must be directly biased and the output reset is connected to phase 3. The variable clamp levels on the drivers allow flexibility in setting the pulsed levels with adjustable DC sources. Finally, Figure 2.11 shows the 4-phase clock which was constructed according to Reference 3 and was found to perform quite satisfactorily.

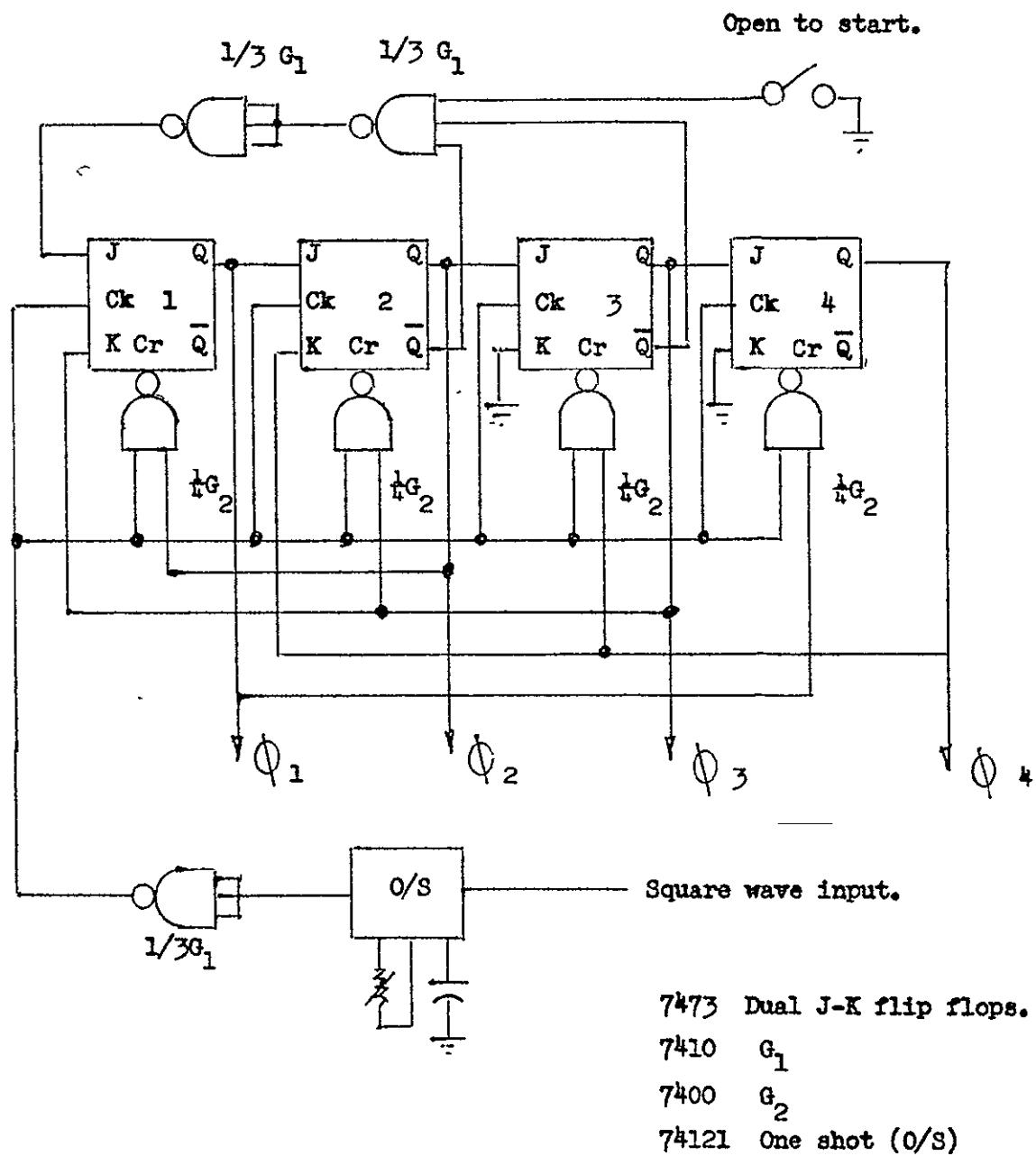


Figure 2.11 Four phase waveform generator adapted from reference 3.

### 3. FABRICATION PROCEDURE

This section describes a nominal fabrication procedure which was used while Section 4 discusses the various modifications which were made. The procedure is very similar to the one reported in References 3 and 4 and was modified to allow incorporation of the input and output gating schemes discussed in the preceding section. Figure 3.1 presents a photomicrograph of a finished CCD which shows the input devices on the left and output devices on the right. The most significant departure from the Texas instruments fabrication procedure reported in the literature<sup>3,4</sup> was that ohmic contact sintering is required after anodization. This is a low temperature (470°C) operation, and the ramifications for this variation are discussed in Section 4.

#### 3.1 Anodization Procedure

This procedure is quite similar to that discussed by Haden, et al.<sup>3</sup> An anodization bath was mixed with 3% tartaric acid mixed in distilled, deionized and filtered water and buffered to a ph of 6 with NH<sub>4</sub>OH. It was then mixed 1:2 with either ethylene glycol or propylene glycol, and most of the results were obtained with the latter. The anodization tank was a stainless steel beaker (~ 500ml) and the aluminum on the wafer was contacted with stainless steel clips, insulated on one side with mylar. A variable power supply capable of over 400V output was used with a milliammeter and a recorder to monitor the current. The anodization procedure was terminated before the observation of the erratic behavior of the current which was described previously.<sup>3</sup> Figure 3.2 shows a recording of the typical current observed during anodization.

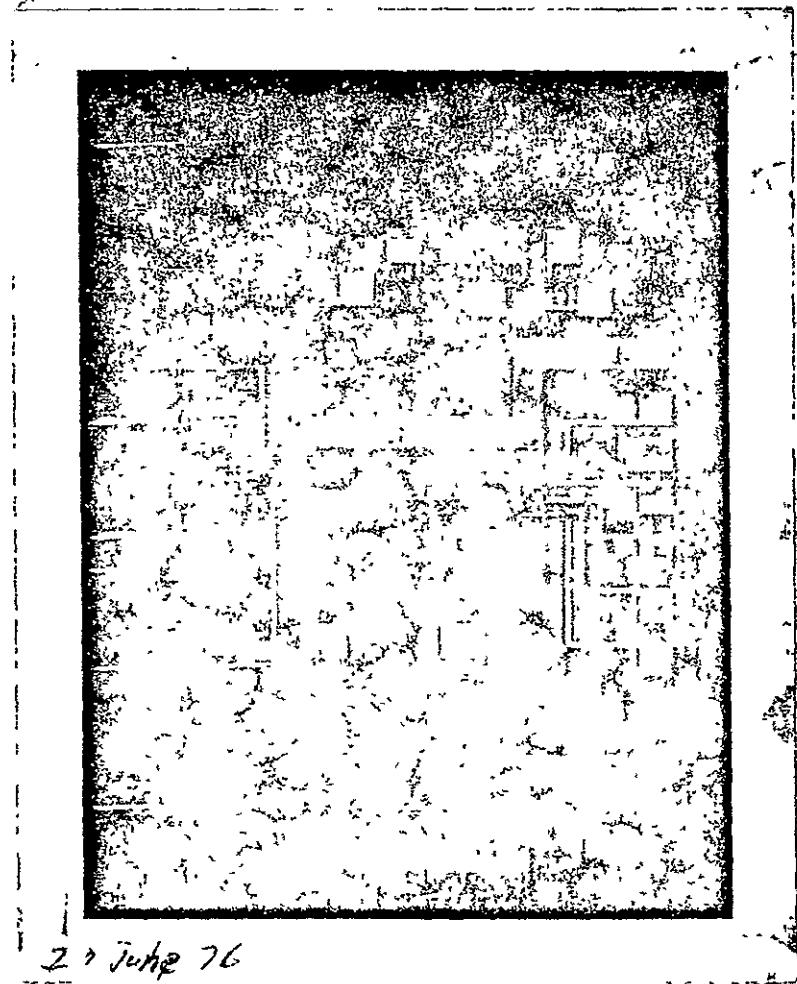


Figure 3.1 Photomicrograph of 4-phase CCD with Al-  
 $Al_2O_3$  insulated gates.

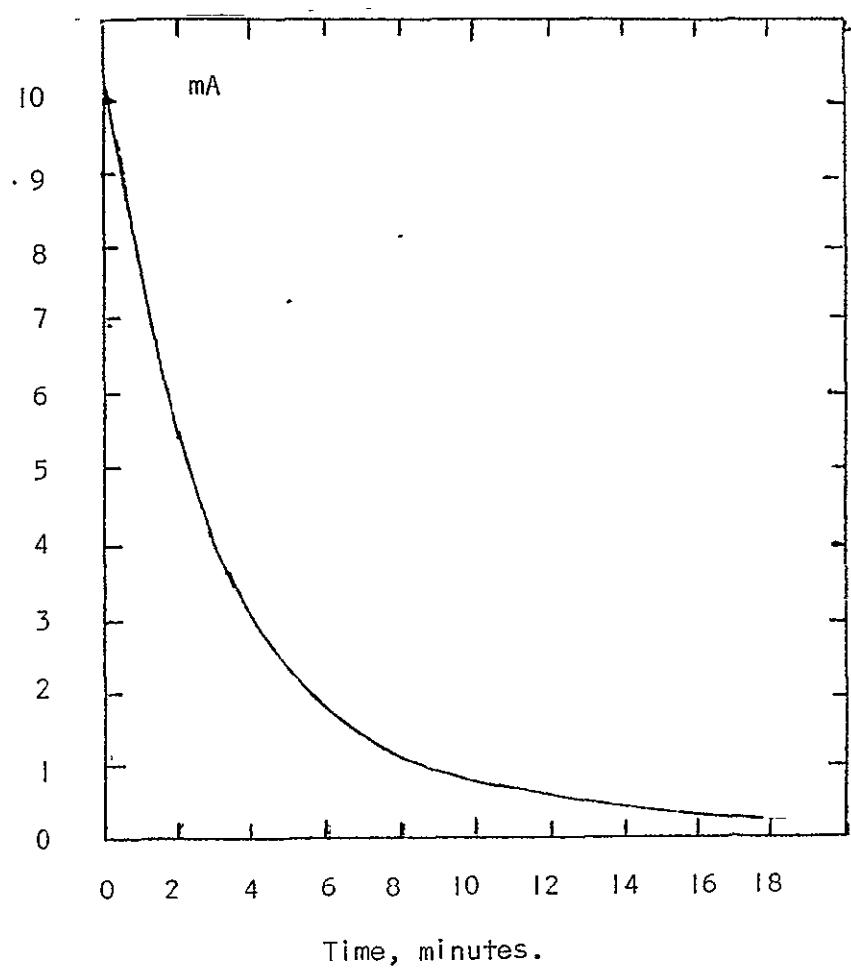


Figure 3.2 Plot of measured anodization current for wafer with devices.

The chemicals used were of the highest quality available with trace impurities at the parts per million level and operations were carried out in a laminar flow hood. Therefore, precautions were taken to insure cleanliness and to avoid contamination.

Most of the work was done using sputtered aluminum; however, as reported in section 4, some of the latter work used thermally evaporated aluminum.

### 3.2 Fabrication Schedule

The remainder of this section gives the process description and shows the mask levels used in processing.

The starting wafers are from Texas Instruments and are <111> silicon, phosphorous doped to 3-5 ohm-cm, and have dislocation densities of < 3000 EP/cm<sup>2</sup>.

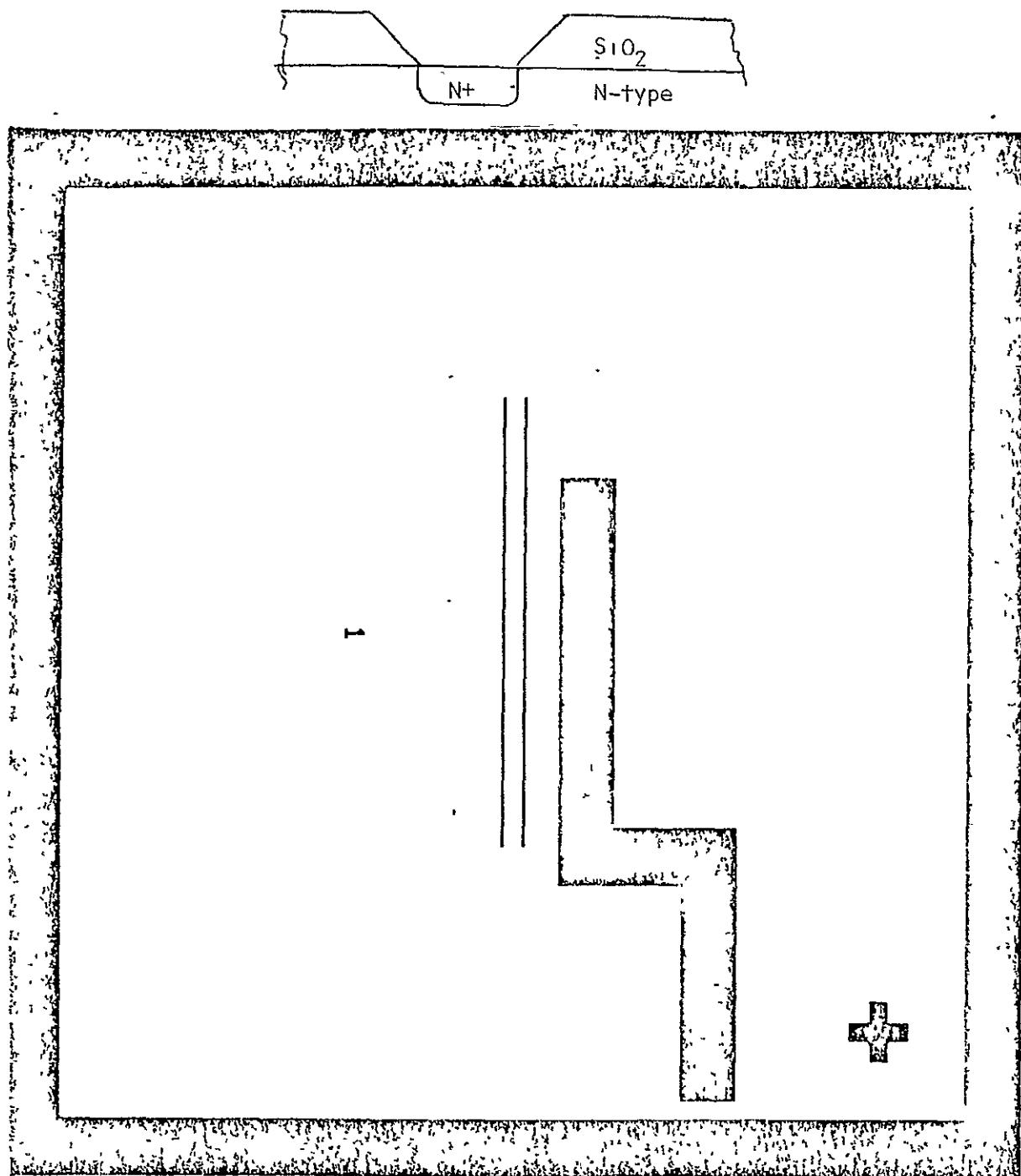
#### A. Wafer clean:

1. DI H<sub>2</sub>O rinse - - - - - 5 min
2. ACE ultrasonic rinse - - - - - 10 sec. dip
3. TCE ultrasonic rinse - - - - - 5 min
4. ACE ultrasonic rinse - - - - - 5 min
5. DI H<sub>2</sub>O rinse - - - - - 10 min
6. H<sub>2</sub>SD<sub>4</sub> - HND<sub>3</sub> (2:1) @ 115°C - - - - - 10 min
7. DI H<sub>2</sub>O rinse - - - - - 10 min
8. Nitrogen blow dry

#### B. Field Oxide Growth, 1200°C:

1. O<sub>2</sub>, 10gb (Matheson 603 rotameter) - - - 10 min
2. Steam, 100°C H<sub>2</sub>O bubble - - - - - 150 min

O<sub>2</sub>, 2 gb(603)



ORIGINAL PAGE IS  
OF 2000 QUALITY

Figure 3.3 First mask level.

3.  $O_2$ , 10 gb (603) - - - - - - - - - - - 10 min

4.  $N_2$ , 10 gb (603) - - - - - - - - - - - 10 min

C.  $N^+$  Diffusion Cutout:

This diffusion is done to create a sharper channel stop than obtained with a thick oxide alone. The mask pattern is shown in Figure 3.3

1. Photoresist application and exposure:

This operation was typically a spin at 6000 rpm for 15 sec of 43 centipoise Kodak resist. The resist was prebaked at 70°C for 20 minutes. Alignment was in a caspar or Electroglas Machine, exposure was for 3 sec and development was done by spraying for 20 seconds. The wafer was rinsed in DI  $H_2O$  and blown or spun dry, inspected under a microscope and post baked at 140°C for 30 minutes.

- o 2. The wafers were then etched in a buffer etch at 50°C for 3 to 3 1/2 minutes. (5 gm  $NH_4F$ : 2cc HF: 8cc DI  $H_2O$ ).
- 3. Rinse in DI  $H_2O$  for 10 minutes.
- 4. Strip photoresist with  $H_2SO_4$ -HNO<sub>3</sub>(2:1) at 115°C, rinse for 10 minutes in DI  $H_2O$ , blow dry with  $N_2$ .

D.  $N^+$  Predeposition at 980°C:

1. DI  $H_2O$  rinse for 5 minutes, blow dry in  $N_2$ .
2. Warmup:  $O_2$ , 4.4 ssb;  $N_2$ , 88 ssb (Brooks R-2-15-A) for 5 minutes.
3. Add:  $PH_3$ , 12 ssb (R-2-15AA);  $N_2$ , 1.5 ssb (R-2-15-A) for 7.5 minutes.
4. Return to warmup condition for 10 minutes (no  $PH_3$ ).

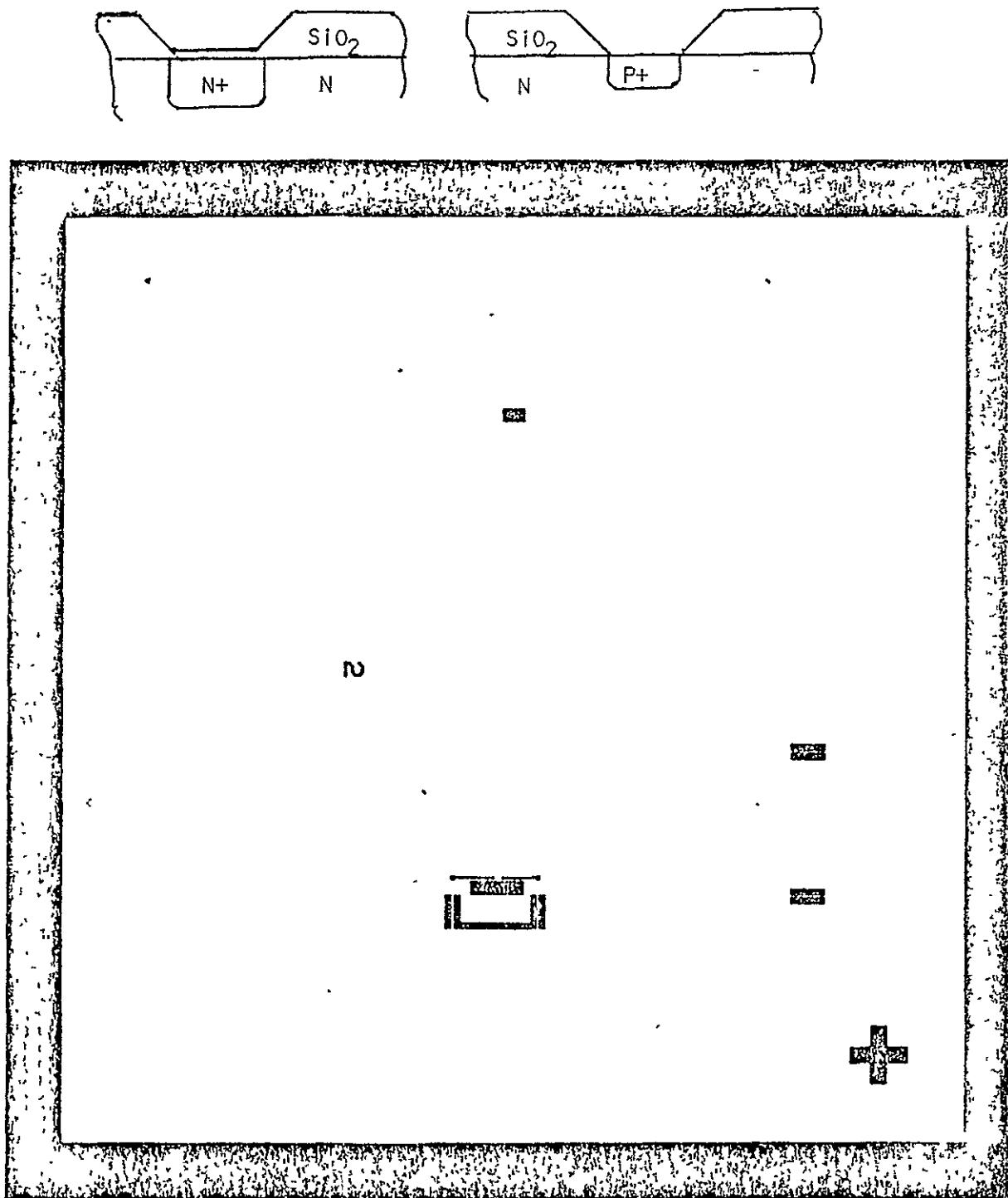


Figure 3.4 Second mask level.

5. Remove phosphorous glass with 10:1 HF etch.
6. Rinse in DI  $H_2O$  for 10 minutes.
7. Check resistivity with 4-point probe for sheet resistance of 16-21 ohms/square.

E.  $N^+$  Drive-in at  $1200^\circ C$ :

This drive-in produces  $2000 \text{ \AA}$  of oxide over the cut-out.

1. Dry  $O_2$ , 10 gb (603) for 10 minutes.
2. Steam, 2 gb (603) bubble, 3 minutes.
3. Dry  $O_2$ , 10 gb (603), 10 minutes.
4.  $N_2$ , 10 gb (603), 10 minutes.

F.  $P^+$  Diffusion Cutout:

This diffusion is done to produce the input and output diodes, the floating diffusion, and the sources and drains of the transistors. The mask is shown in Figure 3.4.

1. Apply standard photoresist procedure as indicated in C.1.
2. Etch in buffer, etch as in C.2.
3. Rinse in DI  $H_2O$  for 10 minutes
4. Remove photoresist as in C.4.

G.  $P^+$  Predeposition at  $980^\circ C$ :

1.  $N_2$ , 10 gb (R-215-B) over boron-nitride doping wafers for 30 minutes.
2. Buffered oxide etch for 1 minute.
3. DI  $H_2O$  rinse for 10 minutes.
4. Jacobsen etch (DI  $H_2O$ : HCl:  $HNO_3$  :  $H_2SO_4$ , 25:5:5:1 of 37% HCl, 70%  $HNO_3$ , 98%  $H_2SO_4$ ) at  $95^\circ C$  for 60 minutes.
5. DI  $H_2O$  rinse for 5 minutes.

ORIGINAL PAGE  
OF POOR QUALITY

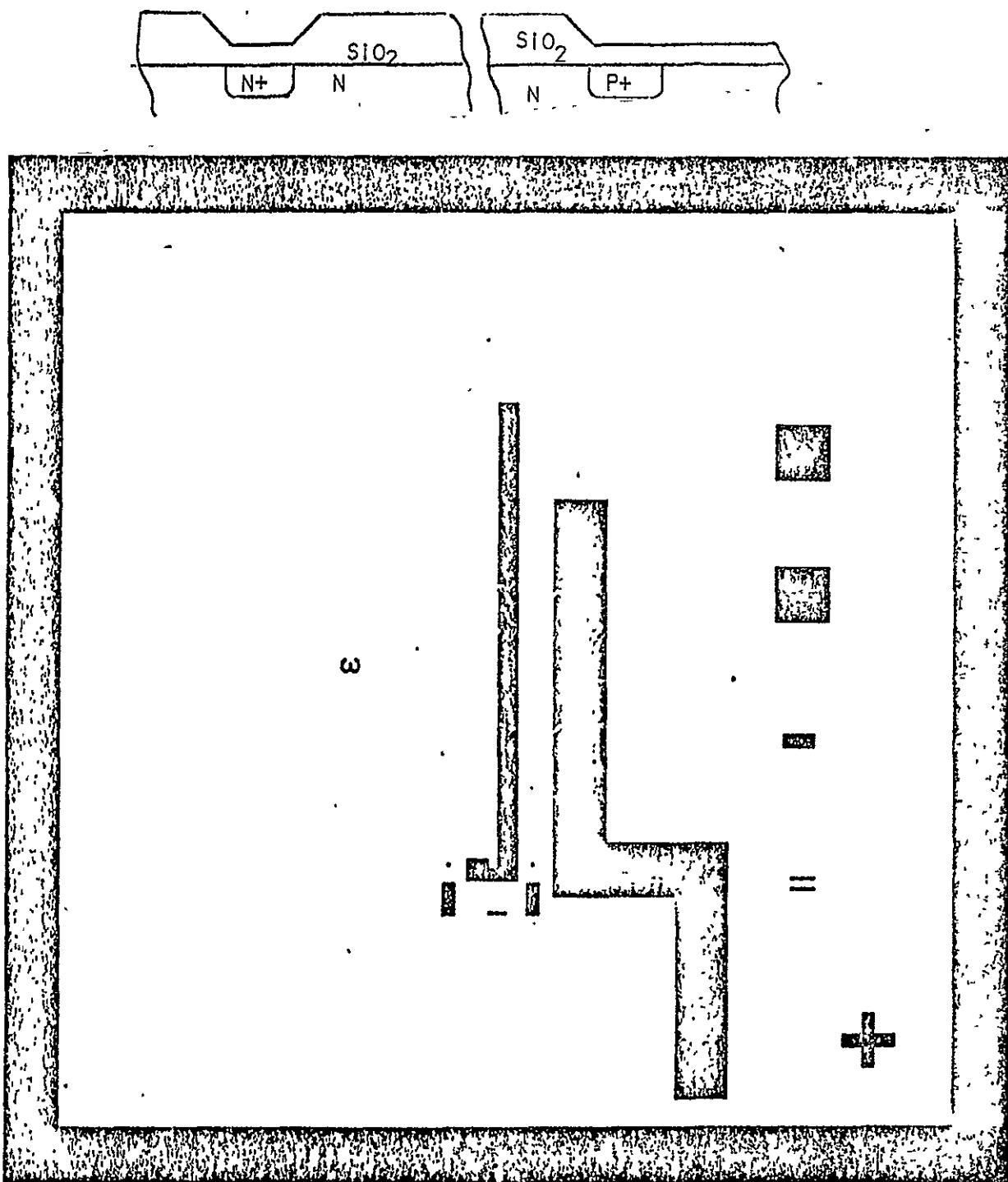


Figure 3.5 Third mask level.

6. Buffered oxide etch for 30 seconds.
7. DI  $H_2O$  rinse for 15 minutes.
8. Furnace dry at  $1000^\circ C$  in  $N_2$ , 15 gb (R2-15-B) for 10 minutes.

H. Gate Oxide Cutout:

This etch forms all of the thin oxide regions for the channels and gates. The mask is shown in Figure 3.5.

1. Apply standard photoresist procedure as in C.1.
2. Buffered oxide etch at  $50^\circ C$  for 3 minutes.
3. Remove photo resist.
4. Measure sheet resistance, 36 ohms/square.

I. Gate oxidation at  $1200^\circ C$ :

1. Etch in  $HNO_3$  at  $85^\circ C$  for 20 minutes
2. DI  $H_2O$  rinse for 10 minutes
3.  $N_2$  blow dry.
4.  $O_2$ , 10 gb (603) for 30 minutes.
5.  $N_2$ , 10 gb (603) for 20 minutes.
6. 10:1 HF dip for 30 seconds.
7. Check oxide thickness for  $1150 \text{ \AA}$  with ellipsometer.

An alternate procedure using  $HCl$  steam for the gate oxide was used on some runs.

J. First Aluminum:

This aluminum was applied by low voltage DC sputtering in Argon.

1. Etch in 10:1 HF for approximately 1-minute.
2. Rinse in DI  $H_2O$  for 15 minutes.
3. Blow dry  $N_2$ .
4. Deposit  $5000 \text{ \AA}$  of aluminum.

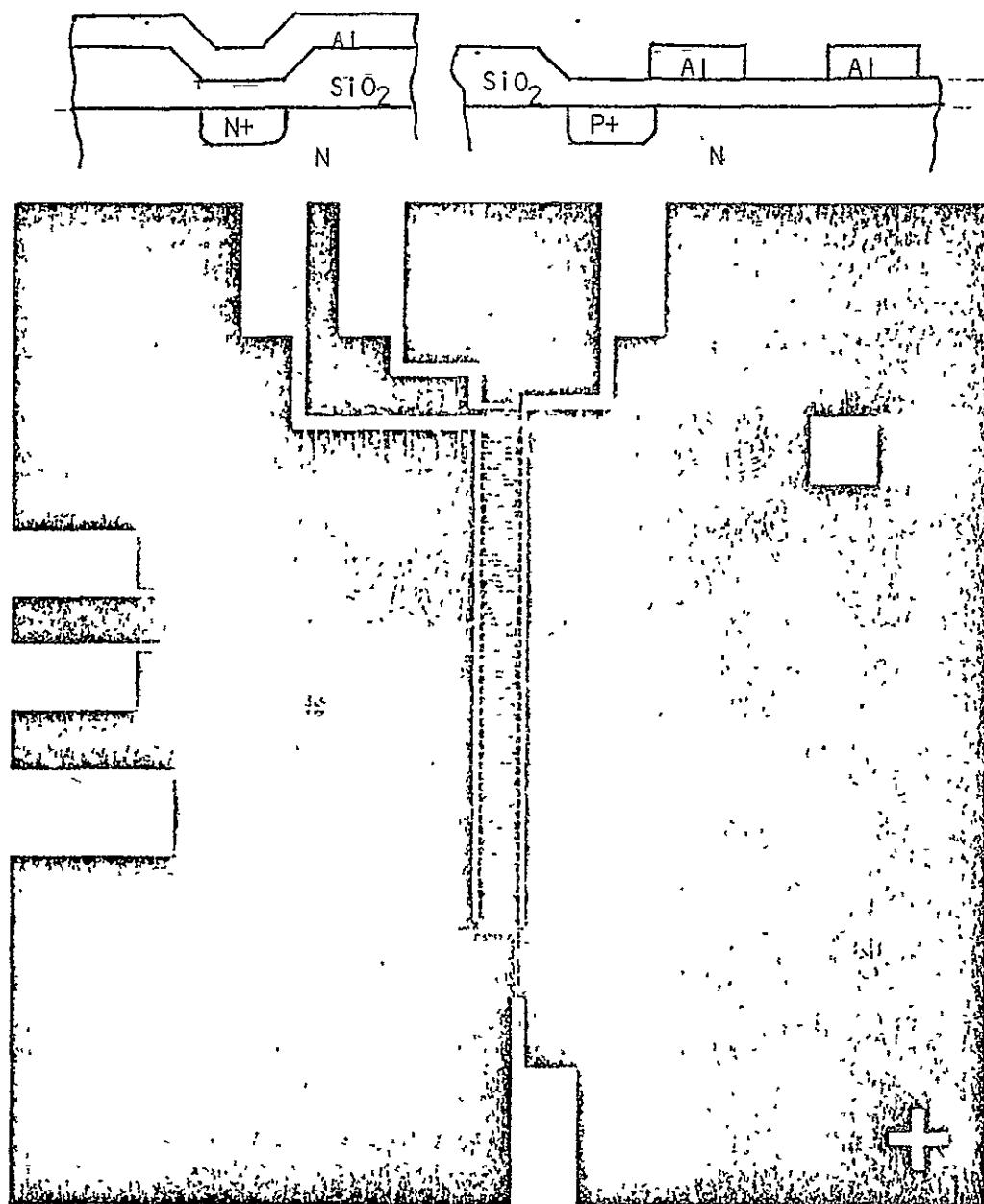


Figure 3.6 Fourth mask level.

K. First Aluminum Etch:

This etch defines all the electrode edges which are incorporated in the charge transfer structure and the bus lines which are used in the anodization procedure. The mask pattern is shown in Figure 3.6.

1. Apply photoresist procedure as in C.1.
2. Etch in  $H_3PO_4$ :  $HNO_3$ : HAC (25:1:5) at  $55^\circ C$  for approximately 70 seconds.
3. DI  $H_2O$  rinse for 10 minutes.
4. Strip photoresist with metal compatible process, chromic-sulfuric acid (1:55), for 30 minutes at room temperature, rinse with DI  $H_2O$  15 minutes and blow dry.
5. Sinter in  $N_2$  at  $470^\circ C$  for 10 minutes.

L. Aluminum Anodization:

1. Rinse in DI  $H_2O$  for 10 minutes.
2.  $N_2$  blow dry.
3. Anodize according to procedure described in Section 3.1.
4. Rinse in DI  $H_2O$  for 10 minutes.
5.  $N_2$  blow dry.
6. Inspect under microscope.

M. Aluminum Oxide Etch:

This procedure is the first departure from that previously published. Connections required between the first and second levels are obtained by exposing the first level through the oxide. The mask is shown in Figure 3.7, and it is seen that that this operation involving etching only near the bonding pads and is not critical.

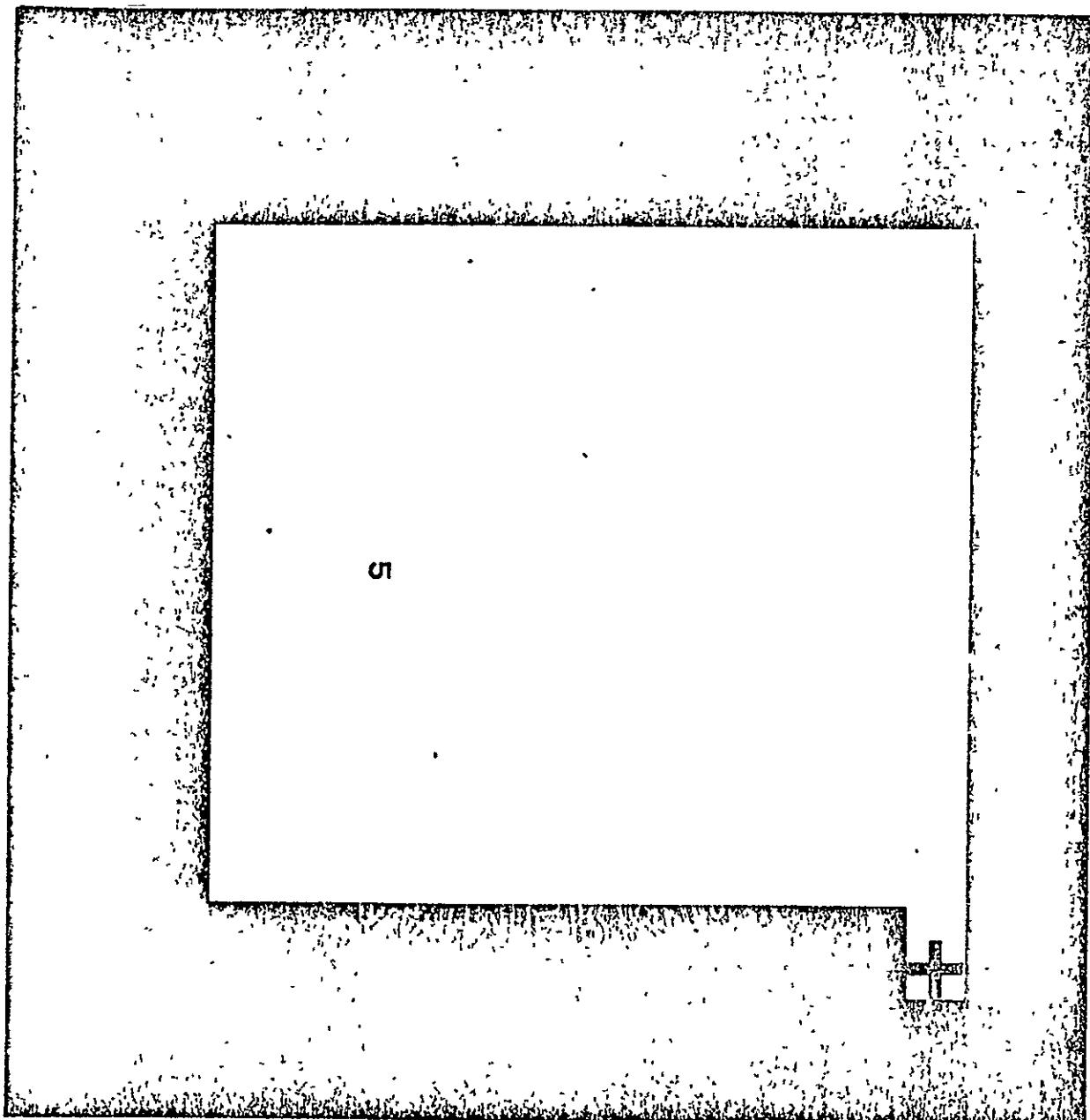
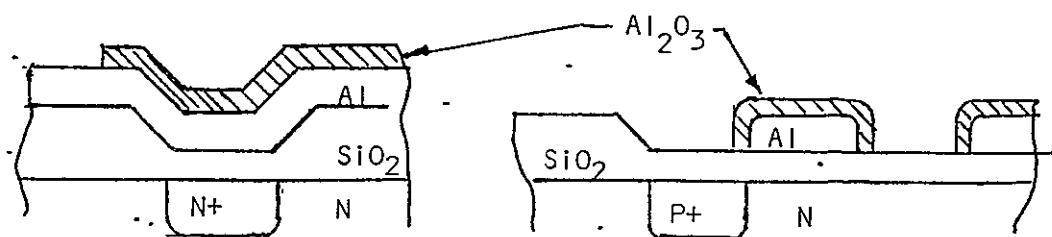


Figure 3.7 Fifth mask level.

ORIGINAL PAGE IS  
OF POOR QUALITY

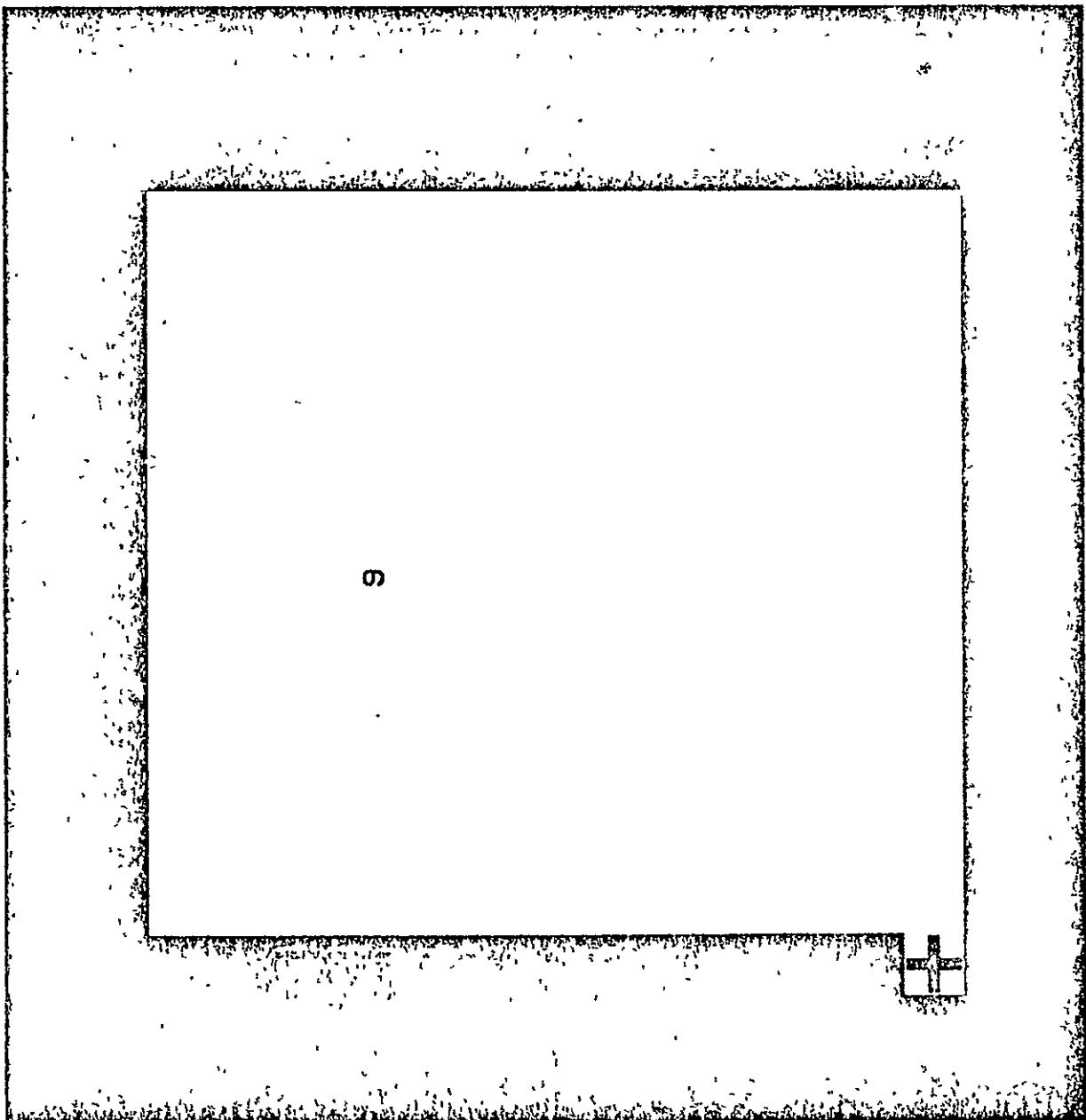
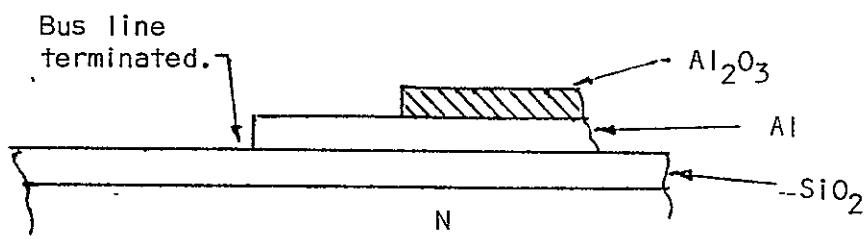


Figure 3.8 Sixth mask level.

1. Dry at 470°C in nitrogen for 10 minutes.
2. Apply photoresist procedure as in C.1.
3. Apply aluminum oxide etch at 100°C for 2 minutes. This etch is composed of 20 gm CrO<sub>3</sub> and 35 mls of 85% HNO<sub>3</sub> diluted in 1000 mls of DI H<sub>2</sub>O.
4. Rinse in DI H<sub>2</sub>O for 15 minutes.
5. Strip photoresist with metal compatible procedure (K.4).
6. Rinse in DI H<sub>2</sub>O for 10 minutes
7. N<sub>2</sub> blow dry and microscope inspection

N. Aluminum Bus Line Etch:

The mask for this procedure is shown in Figure 3.8.

1. Dry in N<sub>2</sub> at 470°C for 10 minutes.
2. Apply photoresist procedure as in C.1.
3. Etch aluminum as in K.2.
4. Strip photoresist with metal compatible procedure as in K.4.
5. Rinse in DI H<sub>2</sub>O for 15 minutes.
6. N<sub>2</sub> blow dry and microscope inspection.

O. Ohmic Contact Cutout:

The mask for this procedure is shown in Figure 3.9.

1. Dry in N<sub>2</sub> at 470°C for 10 minutes.
2. Apply photoresist procedure as in C.1.
3. Do oxide etch in buffer etch at room temperature for approximately 3 minutes.
4. Rinse in DI H<sub>2</sub>O for 10 minutes.
5. Strip photoresist as in K.4.

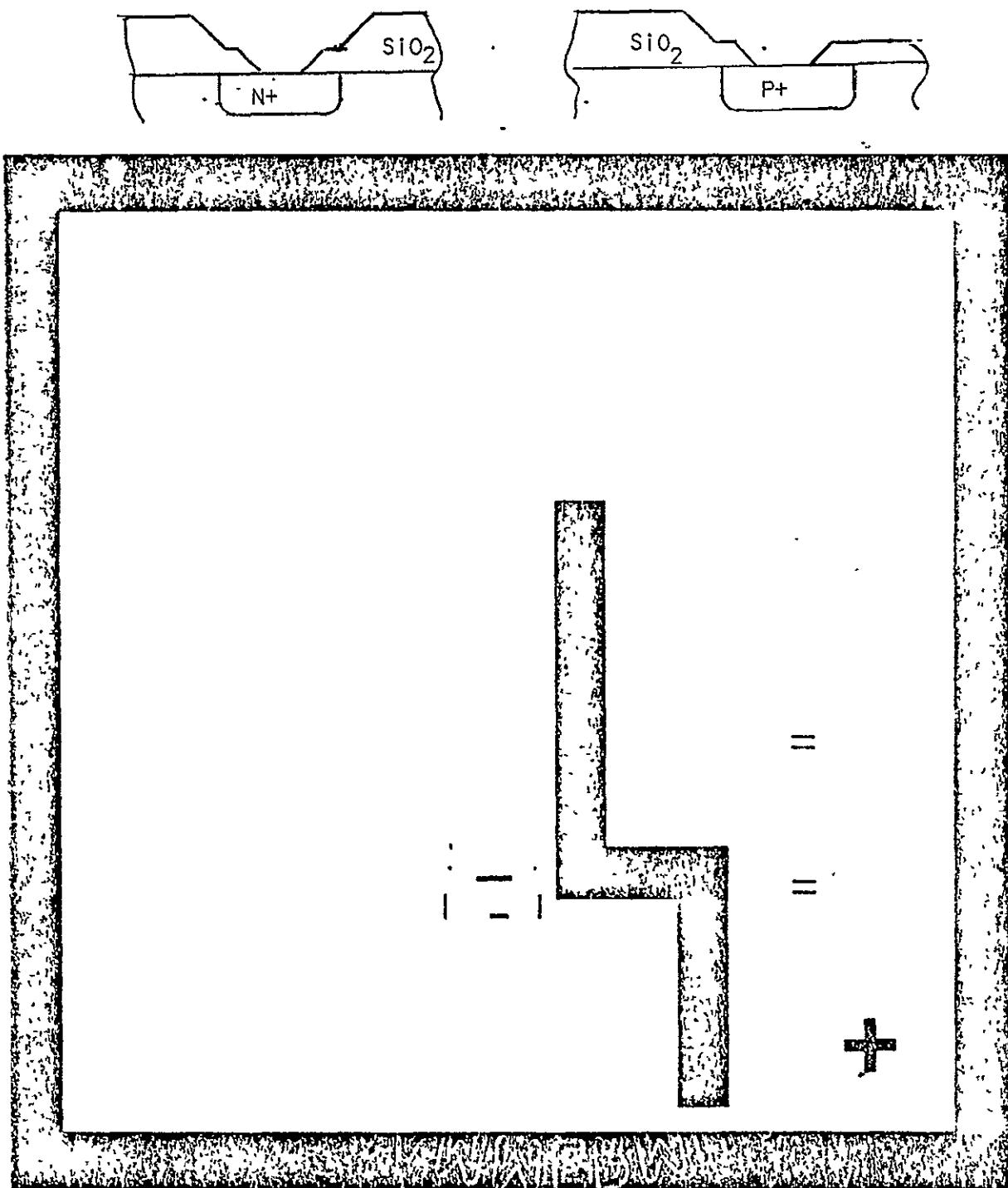


Figure 3.9 Seventh mask level.

REPRODUCED  
FROM ORIGINAL

6. Rinse in DI H<sub>2</sub>O for 15 minutes.
7. N<sub>2</sub> blow dry and microscope inspection.
8. Check final P<sup>+</sup> sheet resistance on test wafers, ohms/square.

P. Second Aluminum Deposition:

1. Etch in 10:1 HF dip for 10 seconds.
2. Rinse in DI H<sub>2</sub>O for 15 minutes.
3. N<sub>2</sub> blow dry.
4. Sputter 5000 Å of aluminum.

Q. Second Aluminum Etch:

The mask for this step is shown in Figure 3.10.

1. Dry for 10 minutes at 140°C.
2. Apply photoresist procedure as in C<sub>1</sub>.
3. Etch in aluminum etch as in K.2.
4. Rinse in DI H<sub>2</sub>O for 10 minutes.
5. Strip photoresist with metal compatible procedure as in K.4.
6. Rinse in DI H<sub>2</sub>O for 10 minutes.
7. N<sub>2</sub> blow dry and microscope inspection.
8. Sinter in N<sub>2</sub> at 470°C for 20 minutes.

R. Optional Passivation Step:

1. Deposit 6000 Å SiO<sub>2</sub> in silox system at approximately 500°C.
2. Apply photoresist procedure, mask number 9, Figure 3.11.
3. Etch with HAC:NH<sub>4</sub>F 40%: H<sub>2</sub>O (1:1:1) for 3 minutes.

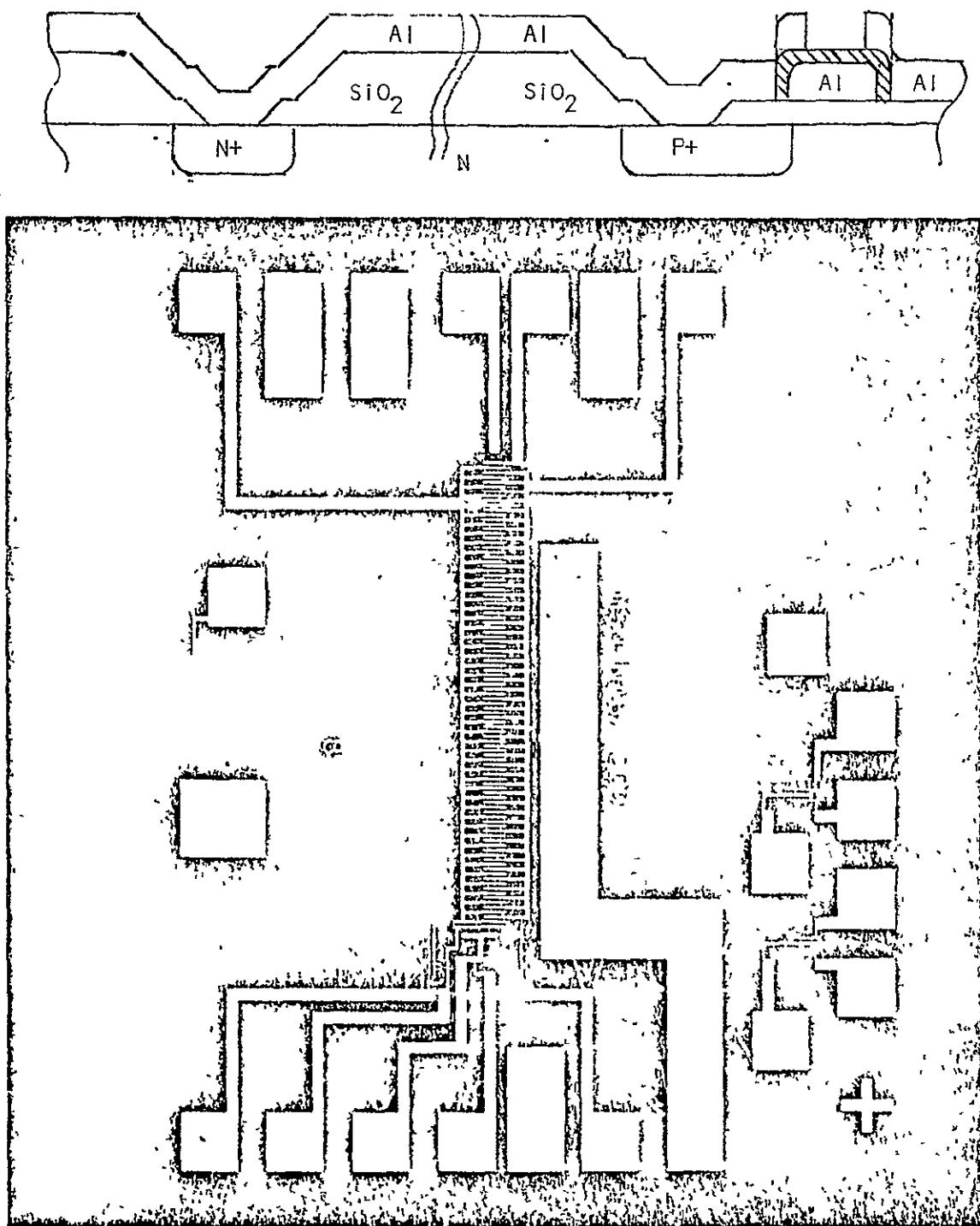


Figure 3.10 Eighth mask level.

REPRODUCIBILITY OF THE  
ORIGINAL PAGE IS POOR

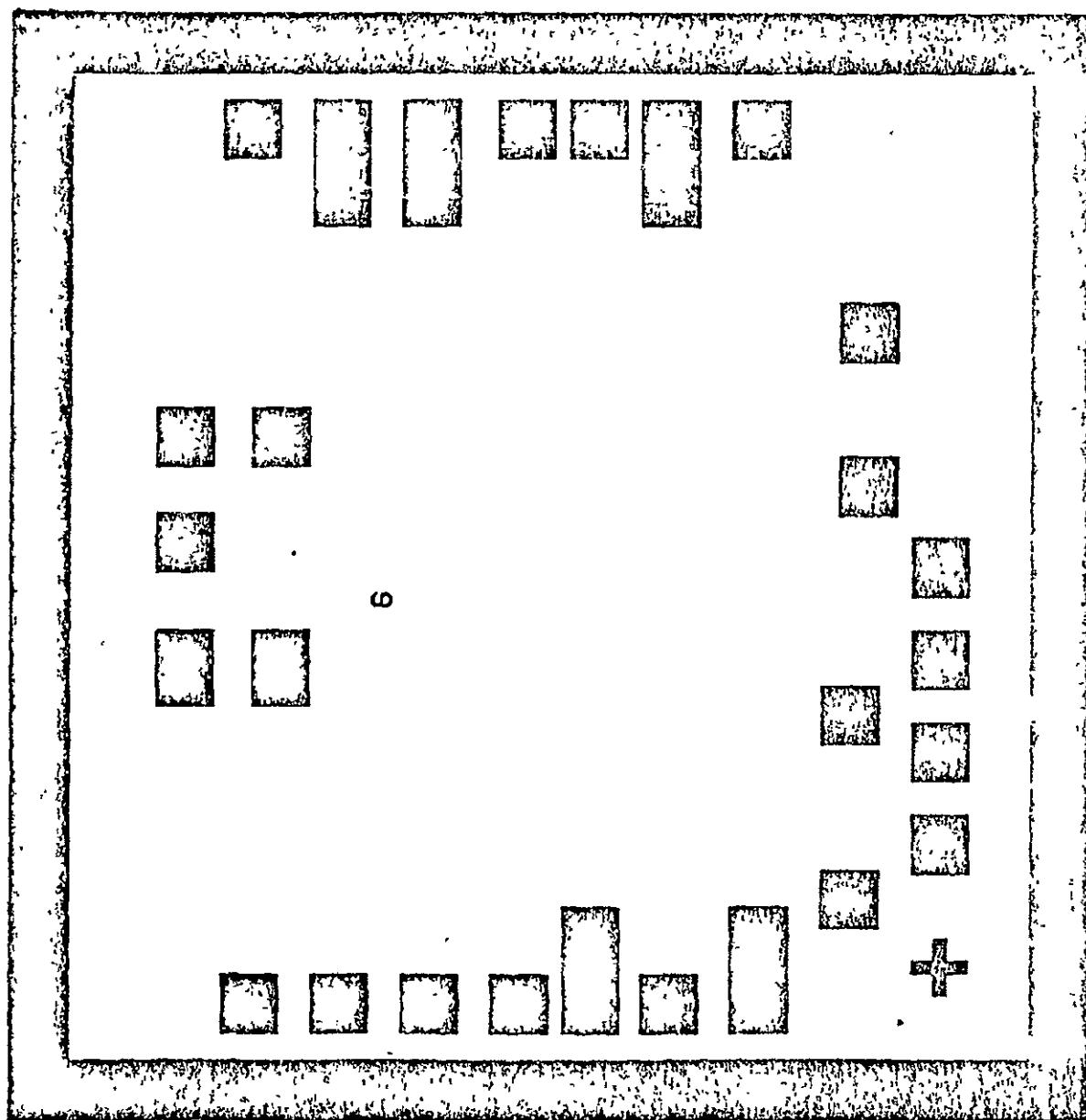


Figure 3.11 Ninth mask level (optional).

#### 4. EVALUATION AND MODIFICATIONS

The fabrication of the devices was accomplished during two periods when access was provided to the facilities at Marshall Space Flight Center for performing the thermal processing and preparing the sputtered aluminum. The preparation and patterning of evaporated aluminum was done at Mississippi State. The following describes the various phases of fabrication and evaluation.

##### 4.1 Initial Run

The first devices were prepared as indicated in Section 3 excepting that ethylene glycol was used as a dilutant in the anodization bath which was not considered to be a critical change. The anodization was done at 200 volts which gave approximately 2000 Å as measured with an ellipsometer, in agreement with the reported oxide growth rate of 10 Å/V. The devices were immediately tested for shorts in the metal and for junction operation using a curve tracer at low voltage. A visual inspection eliminated many devices due to failure of the photoresist; however, approximately half of the devices survived these tests. The wafers were stored in a dust tight box and transported to the MSU labs for further testing. They were re-checked within a month with the same test and approximately twenty percent survived, and, during this test, the wafers were mapped. Approximately two months later the devices were again removed from storage, this time for charge transfer tests; however, the preliminary test was rerun. During this test, all devices exhibited shorts through the anodic oxide at some

point. There was no apparent logic in the failures. On some devices two phase lines would be shorted and on others perhaps the input or output gates were observed to be shorted. It should have been expected that failures on the phase lines would be most numerous since more contact periphery was involved. It seemed clear that the failure was a progressive phenomena. Also, most of the work was done during a summer and fall period when the humidity was high so that static electricity was less of a problem.

The most suspicion was focused on two points. First, although the surface appearance of sputtered aluminum is markedly superior to evaporated aluminum with respect to smoothness on a large scale, the sputtered aluminum has some texture. The second point of suspicion was that the anodic oxide was affected during sintering and drying.

#### 4.2 Thermally Evaporated Aluminum.

---

This run used the previous wafers which were stripped back during three etching steps, one for the aluminum oxide and two for aluminum. The same masks were used as previously so that the same patterns were formed. Drying before photoresist application was done at approximately 70°C and separate experiments with sintering suggested that the sintering step should be eliminated to get a check on the insulation without this complication. The anodization bath was modified to use the originally reported propylene glycol dilutant.

These devices were checked after the above procedure and all failed the insulation tests. Separate patterns of large area (100 x 100 mils) capacitors were prepared on silicon wafers cleaned but otherwise unprocessed. None of the capacitors survived the insulation tests. In this

case there was no sharp edge effect and blunt probes were used to prevent punching through the insulation. All of the capacitors were shorted.

#### 4.3 Additional Runs with Sputtered Aluminum

In these runs, wafers were processed with several modifications as well as by the standard procedure:

- (a) Anodized oxides were prepared with 2000, 3000, and 4000 Å to determine the role of thickness.
- (b) Microstrip was used for photoresist removal for all work after any aluminum was in place.
- (c) Drying before photoresist application was done using HMDS and 140°C bake to eliminate drying at higher temperatures.
- (d) The second sintering step was omitted.
- (e) Finally, anodization was done on assputtered aluminum with no sintering operations done at all.

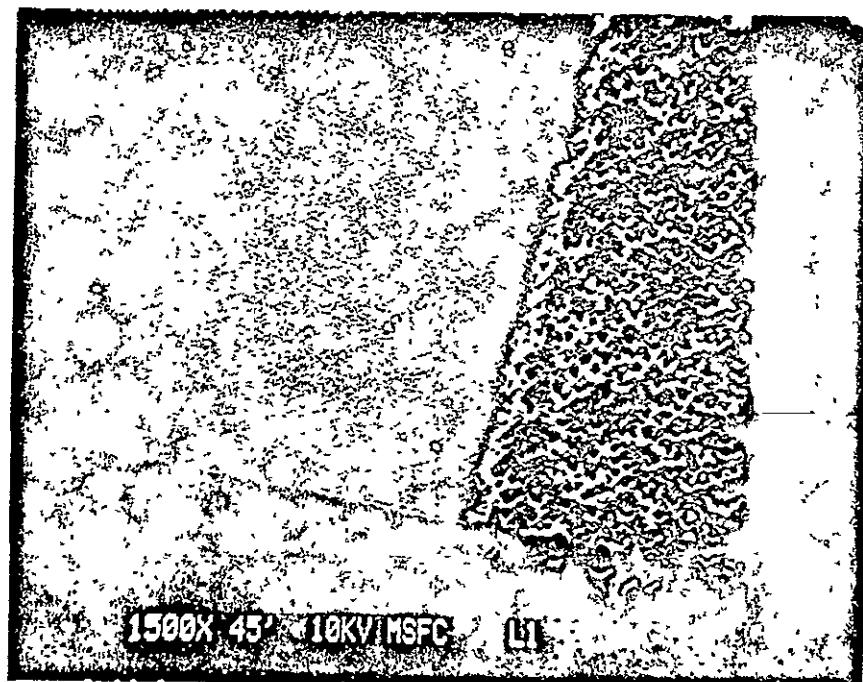
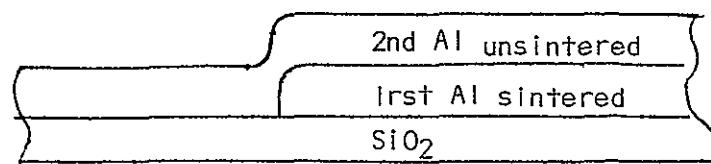
In every case, there was one hundred percent failure in that every device had at least one short. Therefore it appeared that the failure was not caused primarily by too thin of an oxide, by inadvertent etching during photoresist stripping, nor due to thermally induced effects during drying and sintering.

#### 4.4 SEM Inspections.

Figure 4.1 shows a SEM image of the boundary of the connection between the top and bottom levels which occurs near a bonding pad. The cross-sectional drawing indicates the configuration where second level metal crosses over first level without an oxide between. One may note that the sputtered aluminum on  $SiO_2$  to the left has the smooth surface and good etch definition which is characteristic of this technique of

REPRODUCIBILITY OF THE  
ORIGINAL PAGE IS POOR

48



24 July

Figure 4.1 SEM image of unsintered sputtered aluminum on  $\text{SiO}_2$  and sputtered, sintered aluminum.

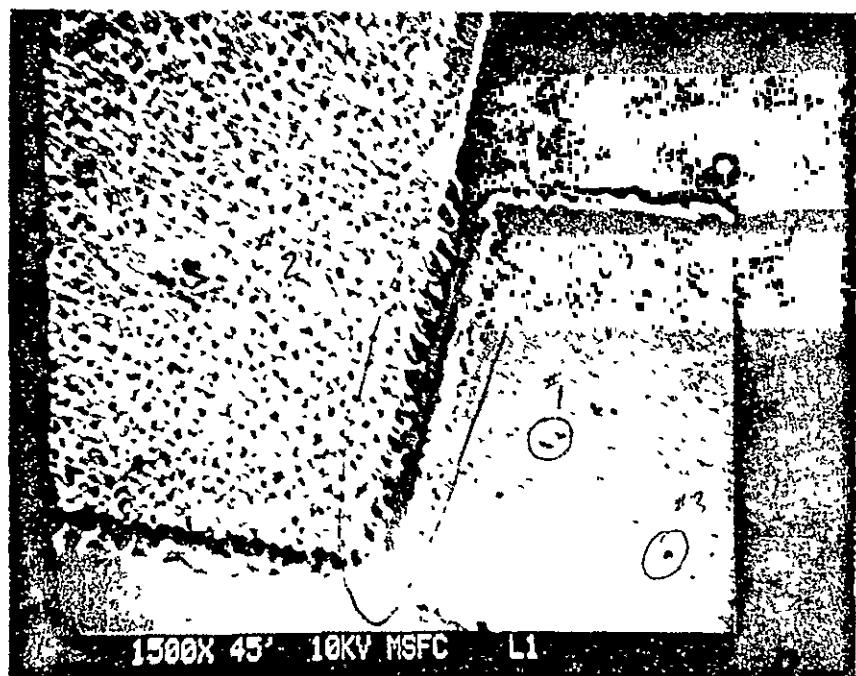
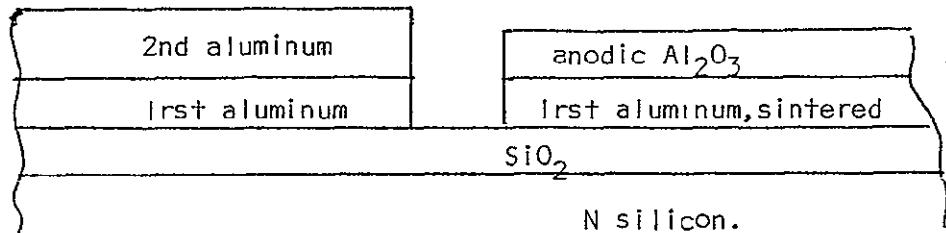
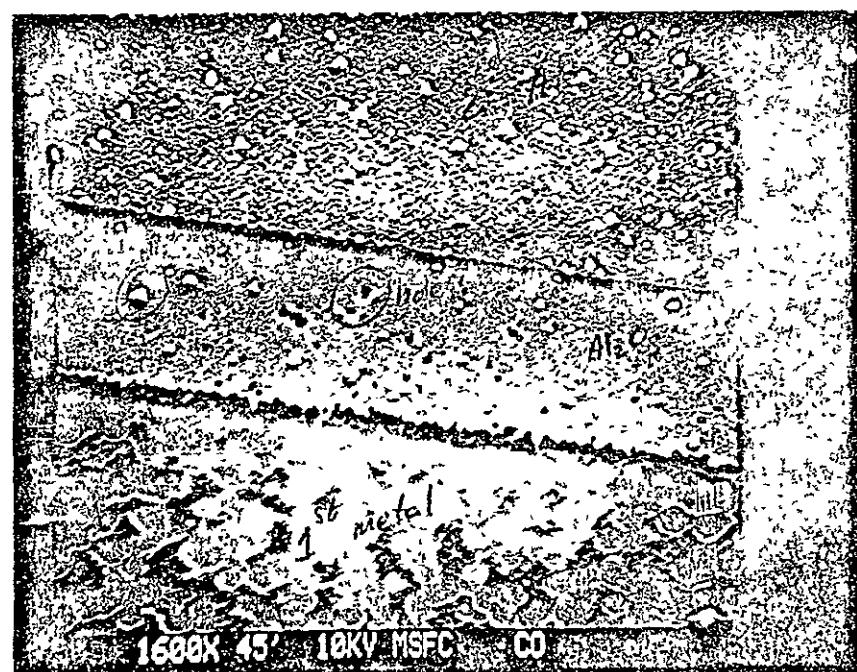
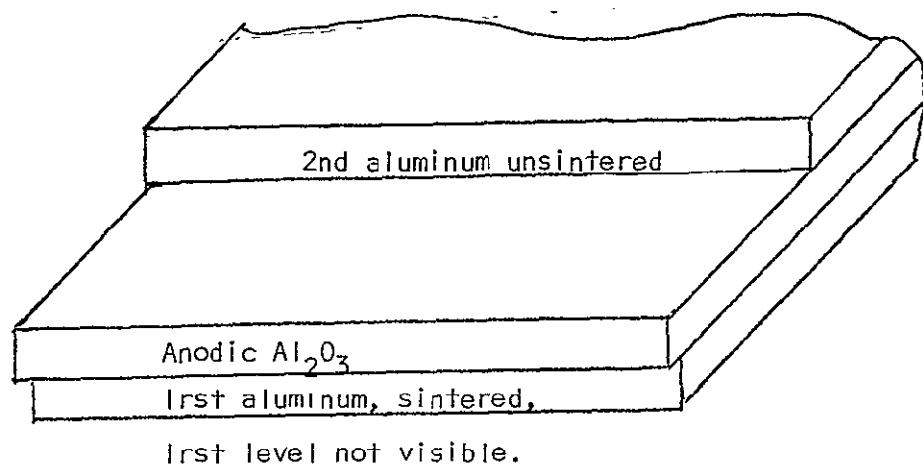


Figure 4.2 SEM image of unsintered, sputtered aluminum on sintered aluminum and anodic  $\text{Al}_2\text{O}_3$  on sintered aluminum.

REPRODUCIBILITY OF THE  
ORIGINAL PAGE IS POOR

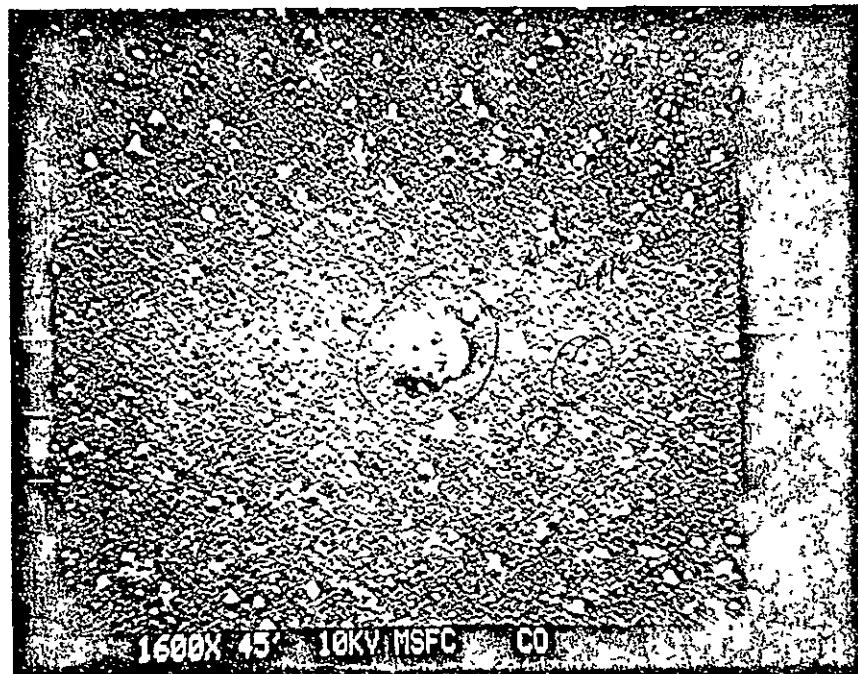
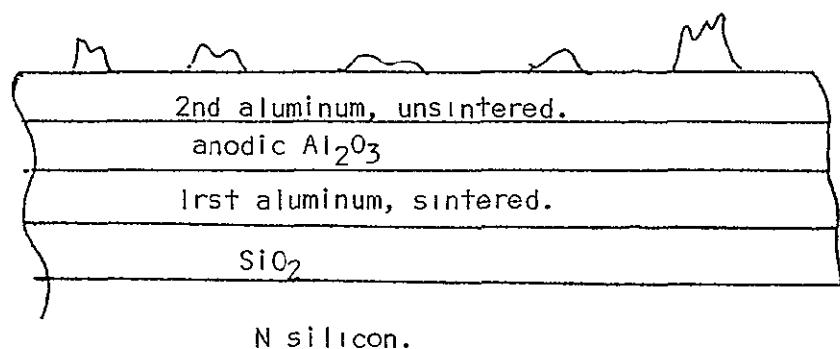
,50



297

Figure 4.3 Stepped SEM image of unsintered, sputtered  
aluminum on anodic  $\text{Al}_2\text{O}_3$  on sintered aluminum.

Hillocks (protuberances)



27

Figure 4.4 Normal SEM image of unsintered, sputtered aluminum on anodic  $\text{Al}_2\text{O}_3$  on sintered aluminum.

metallization. The same layer sputtered over previously sputtered and sintered aluminum has a spongy appearance with poor etch definition.

Figure 4.2 shows another image on a pad where mask error had produced cleavage of a line. The spongy textured aluminum to the left is a second level layer sputtered over first layer aluminum. To the right, one sees the anodized oxide. There appear to be small protuberances as well as indentations in the oxide.

Figure 4.3 shows another view of second level aluminum over anodized oxide. At the bottom of the picture there appear to be remnants of the first level metal left after etching. This etching of the first level test transistor pads was a consequence of a mask error which inadvertently removed the protective  $\text{Al}_2\text{O}_3$ . Again there appear to be both protuberances and indentations in the anodic oxide. On the second level metal, there appear to be protuberances such as have been observed in metal migration studies.

Figure 4.4 shows an image of second level metal over anodic oxide in a region removed from an etched edge. This image shows a wider distribution in the sizes of the protuberances than in Figure 4.3. A similar observation was made on thermally evaporated aluminum. C

None of the observations give an obvious explanation of the failures. Perhaps the most plausible explanation is that the larger protuberances represent a bridge in which metal has pushed up from the first level through the nodic oxide. From both SEM images and optical microscope examinations, it appears that the protuberances (hillocks) grow during processing from very small nucleation sites such as appear on the left side area in Figure 4.1. The growth seems to be accelerated during sintering operations.

## 5. SUMMARY AND CONCLUSIONS

The accomplishments of tasks in this work were:

1. A numerical analysis was made of MOS-RC transmission line structures including a depletion layer capacitance in series with the oxide capacitance. The rise time at the open end of the line was obtained as a function of averaged sheet resistivity, capacitance, and amount by which the voltage exceeds the threshold value. The rise time is indicative of the limitation in the speed of operation which may be encountered in CCD operation, and it is a function of the ratio of the square of the length of the line to the mobility and of the voltage for voltage levels above the threshold value.
2. The electrical design for a 49 1/2 bit CCD with a low noise input circuit and floating diffusion, or balanced gated charge integration output detector, was achieved using a 4-phase scheme based upon anodized aluminum insulation. Clock and driver circuits for testing the CCDs were also designed and constructed.
3. The masks were designed for the photolithographic procedures used in the fabrication of the CCDs.
4. A fabrication procedure was developed which was based upon a modified P-channel MOS process and previously reported procedures for anodization of aluminum.
5. Four different runs were made in which both sputtered and thermally evaporated aluminum metallizations were prepared.

Several variations were made in the drying procedures before stripping, and in the metal sintering. Twenty wafers were carried through full processing and two were reprocessed with respect to metallization.

6. Electrical insulation tests, visual inspections and SEM studies were made on the devices.

The conclusions based upon this work are:

1. Electrical insulation failures occurred at some point on all devices which were fabricated.
2. The cause of failure could not be directly associated with drying and sintering procedures, the metal deposition scheme, the photoresist stripping procedure, noredge effects at overlapping transfer gates. The aluminum oxide etching was done only near the chip edges as was the bus line etching and neither were believed to be the source of the problem.
3. SEM studies showed that the texture of the sputtered metal is changed rather dramatically in a 470°C sintering operation in  $N_2$ . Therefore, sintering and drying at this temperature should be avoided after anodization. The texture of unsintered sputtered aluminum over anodized sintered aluminum also is rather porous looking but not as much so as over unanodized aluminum.
4. The most likely source of failures appears to be the occurrence of hillocks of aluminum which may protude up from the first level of metallization through the second level. Even if these hillocks are insulated during the anodization procedure, they would represent high stress points for concentration of the

electric field and might fail under low voltage conditions.

These hillocks were observed on both sintered and un-sintered metal and on sputtered and evaporated aluminum.

The recommendations based upon this work are:

1. One should not anticipate reliable CCDs fabricated using the procedures for anodization of deposited aluminum which have been reported in the literature. The techniques for metal preparation for reliable results have not been reported and are apparently critical and subtle. It is also conceivable that successful devices have been obtained from very low yield processes.
2. Although the effect of temperature as a primary source of failure could not be established, it is apparent that the processing in  $N_2$  at  $470^\circ C$  dramatically affects the sputtered aluminum texture. Therefore, anodized aluminum structures should be prepared with three metallizing steps. The first would produce only the ohmic contacts after which sintering would be done. After this step the temperature should be kept low during drying operations. It is not known what the critical temperature value is. The second step would produce the bottom level in the sandwich structure and would be followed by the anodization and second level deposition.
3. The attractiveness of all aluminum phase structures for CCDs is indisputable. For some applications of CCDs which are most demanding in terms of speed, the polysilicon phase line, if used, will limit the ultimate speed. Therefore fundamental

research for the development of a reliable metallization and anodization scheme which is compatible with silicon integrated circuit technology should be carried out and the results published in order to advance the state of the art in CCD design and fabrication.

## REFERENCES

1. J. D. Gassaway and R. J. Whelchel, "Application of LSI to Signal Detection: The DELTIC DFPCC," Interim NASA report, EIRS-EE-2, Mississippi State University, January 1975.
2. W. R. McMahon and T. H. Ramsey, U. S. Patent No. 3634203, "Thin Film Metallization Processes for Microcircuits," 1972.
3. D. R. Collins, S. R. Shortes, W. R. McMahon, R. C. Bracken, and T. C. Penn, "Charge-coupled Devices Fabricated Using Aluminum-anodized Aluminum-aluminum Double-level Metalization," J. Electrochem Soc., Vol. 120, No. 4, p. 521, 1973.
4. C. R. Haden, J. L. Barrett and J. L. Stone, "High-quality dielectric Suitable for Use with Amorphous Semiconductors," IEEE J. Solid State Circuits, Vol. SC9, No. 3, p. 118, 1974.
5. L. J. M. Esser, "The Peristaltic Charge-coupled Device for High Speed Charge Transfer," Digest of Tech. Papers, IEEE International Solid State Circuits Conference, Phila., February 1974.
6. R. K. Raymond and M. B. Das, "Fabrication and Characteristics of MOS-FETs Incorporating Anodic Aluminum Oxide in the Gate Structure," Solid State Elect., Vol. 19, p. 181, 1976.
7. R. H. Walden (et al.), "The Buried-channel Charge-coupled Device," BSTJ, Vol. 51, No. 7, p. 1635, 1972.
8. M. S. Worley, M.Sc. Thesis, Mississippi State University, (to be published) June 1977.
9. C. H. Chan and S. G. Chamberlain, "Numerical Methods for the Charge Transfer Analysis of Charge-Coupled Devices," Solid State Elect., Vol. 17, p. 491, 1974.
10. R. W. Brodersen (et al.), "Experimental Characterization of Charge Transfer Efficiency in Surface Channel Charge-Coupled Devices," Proceedings, Applications Conference on CCDs, NEL, San Diego, p. 169, 1973.
11. M. F. Thompsett, "Surface Potential Method of Setting Charge in Charge-coupled Devices," IEEE Trans. on Electron Devices, Vol. ED-22, No. 6, 1975.
12. W. F. Kosonocky and J. E. Carnes, "Two-phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," RCA Review, Vol. 34, p. 164, 1973.
13. Fairchild Space and Defense Systems, Report No. ED-AX-16, "Low Light Level Charge-Coupled Imaging Devices," Oct. 1973.